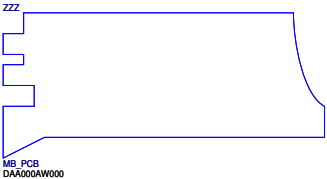


MODEL NAME : *AAZ80*

PCB NO : *LA-C881P*

BOM P/N : *TBD*



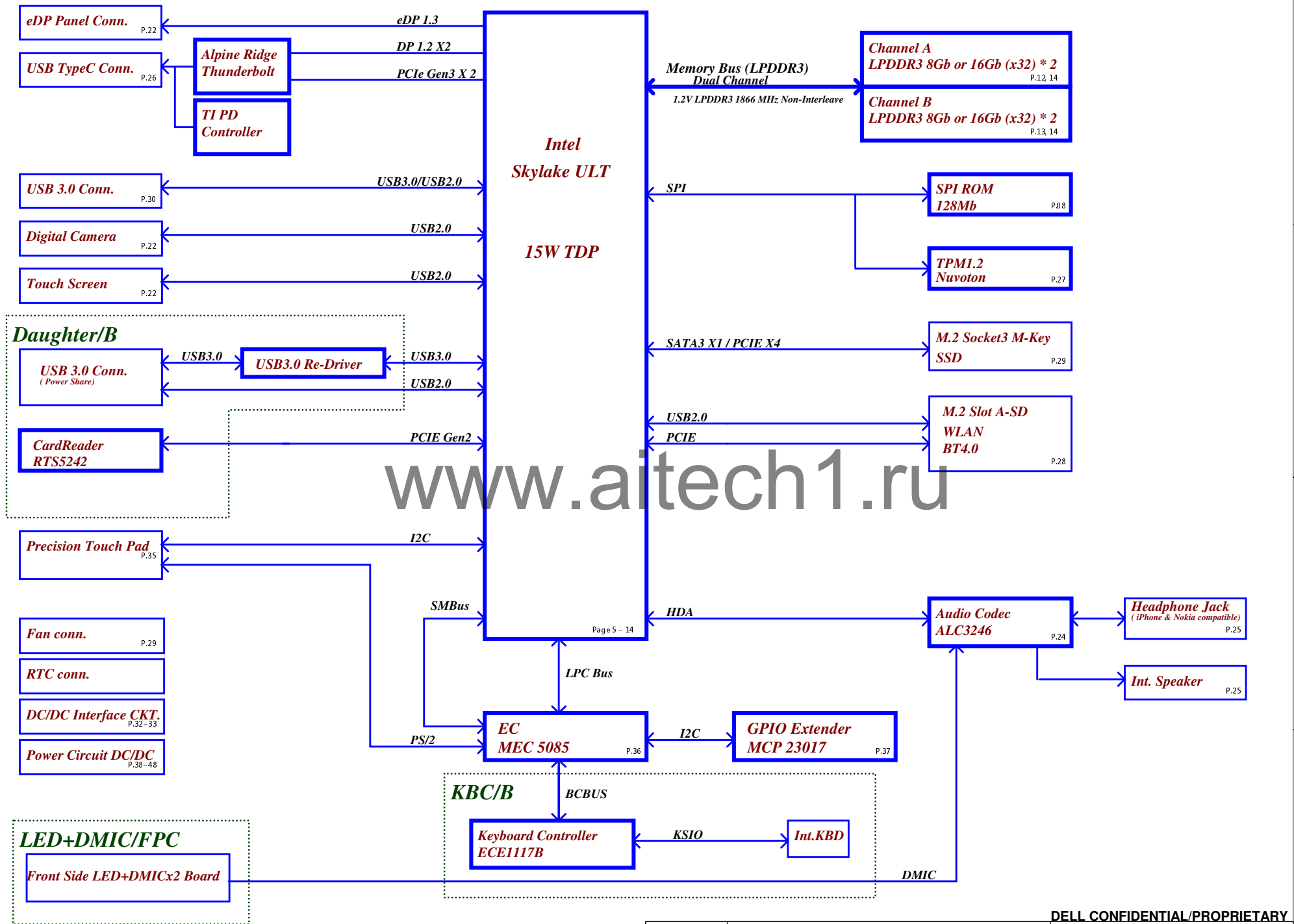
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Dell/Compal Confidential

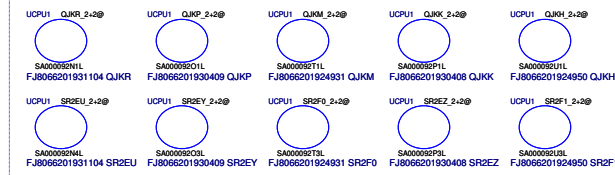
Schematic Document
Dino2 (Skylake ULT)
www.aitech1.ru

2015-09-16

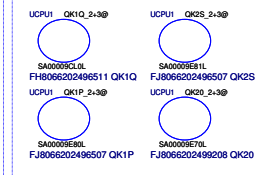
Rev: 1.0 (A00)



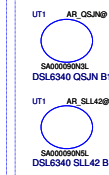
2+2 CPU Option



2+3 CPU Option



AR Option



DRAM Option

	UD19 M1G 1866@	UD20 M1G 1866@	UD21 M1G 1866@	UD22 M1G 1866@	MEM_CONFIG0 RH144 M1G 1866@	MEM_CONFIG1 RH139 M1G 1866@	MEM_CONFIG2 RH145 M1G 1866@	MEM_CONFIG3 RH151 M1G 1866@	MEM_CONFIG4 RH147 M1G 1866@
Micron 4G/1866	SA00008PF1L EDF8132A3MA-JD-F-R A311	SA00008PF1L EDF8132A3MA-JD-F-R A311	SA00008PF1L EDF8132A3MA-JD-F-R A311	SA00008PF1L EDF8132A3MA-JD-F-R A311	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%
Micron 8G/1866	SA00008Q11L EDFA232A2MA-JD-F-R A311	SA00008Q11L EDFA232A2MA-JD-F-R A311	SA00008Q11L EDFA232A2MA-JD-F-R A311	SA00008Q11L EDFA232A2MA-JD-F-R A311	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%
Hynix 4G/1866	SA00008G61L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SA00008G61L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SA00008G61L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SA00008G61L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Hynix 8G/1866	SA00008FJ1L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SA00008FJ1L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SA00008FJ1L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SA00008FJ1L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Samsung 4G/1866	SA00008PO1L K4E8E304EE-EGCF A311	SA00008PO1L K4E8E304EE-EGCF A311	SA00008PO1L K4E8E304EE-EGCF A311	SA00008PO1L K4E8E304EE-EGCF A311	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Samsung 8G/1866	SA00008QV1L K4E8E304EE-EGCF A311	SA00008QV1L K4E8E304EE-EGCF A311	SA00008QV1L K4E8E304EE-EGCF A311	SA00008QV1L K4E8E304EE-EGCF A311	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Micron 16G/1866	SA00008QW1L EDFB232A1MA-JD-F-R A311	SA00008QW1L EDFB232A1MA-JD-F-R A311	SA00008QW1L EDFB232A1MA-JD-F-R A311	SA00008QW1L EDFB232A1MA-JD-F-R A311	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Samsung 16G/2133	SA00008VV1L K4E8E304EB-EGCG A311	SA00008VV1L K4E8E304EB-EGCG A311	SA00008VV1L K4E8E304EB-EGCG A311	SA00008VV1L K4E8E304EB-EGCG A311	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Samsung 16G/1866	SA00008X11L K4E8E304EB-EGCF A311	SA00008X11L K4E8E304EB-EGCF A311	SA00008X11L K4E8E304EB-EGCF A311	SA00008X11L K4E8E304EB-EGCF A311	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Hynix 16G/1866	SA00008Y1L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SA00008Y1L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SA00008Y1L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SA00008Y1L H5CCNNN8GTMLAR-NUD ABBCNNN8GTMLAR-NUD	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D

Board ID Table for AD channel

RE79	CE54	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

	SKU	PTT	TPM2.0
Dino2	Vpro+CS	Disable	Enable
	nVpro+CS	Enable	None

SMBUS Control Table

	SOURCE	23017	BATTERY	Charger	PD	5085	XDP	Audio	Touch Pad
I2C1A_CLK I2C1A_DATA	MEC5085	V							
I2C1C_CLK I2C1C_DATA	MEC5085		V						
I2C1G_CLK I2C1G_DATA	MEC5085			V					
I2C2A_CLK I2C2A_DATA	MEC5085				V				
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH					V			
SMBCLK SMBDATA	PCH						V		
I2C0_CLK I2C0_DATA	PCH								
I2C1_CLK I2C1_DATA	PCH								V


PCH USB 2.0 Port Mapping	USB PORT#	DESTINATION
	1	External USB3(On IOB)
	2	External USB3(On MB)
	3	NGFF CARD WLAN
	4	Touch Panel
	5	Camera
	6	
	7	
PCH USB 3.0 Port Mapping	1	External USB3(On IOB)
	2	External USB3(On MB)


PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
	2	Alpine Ridge

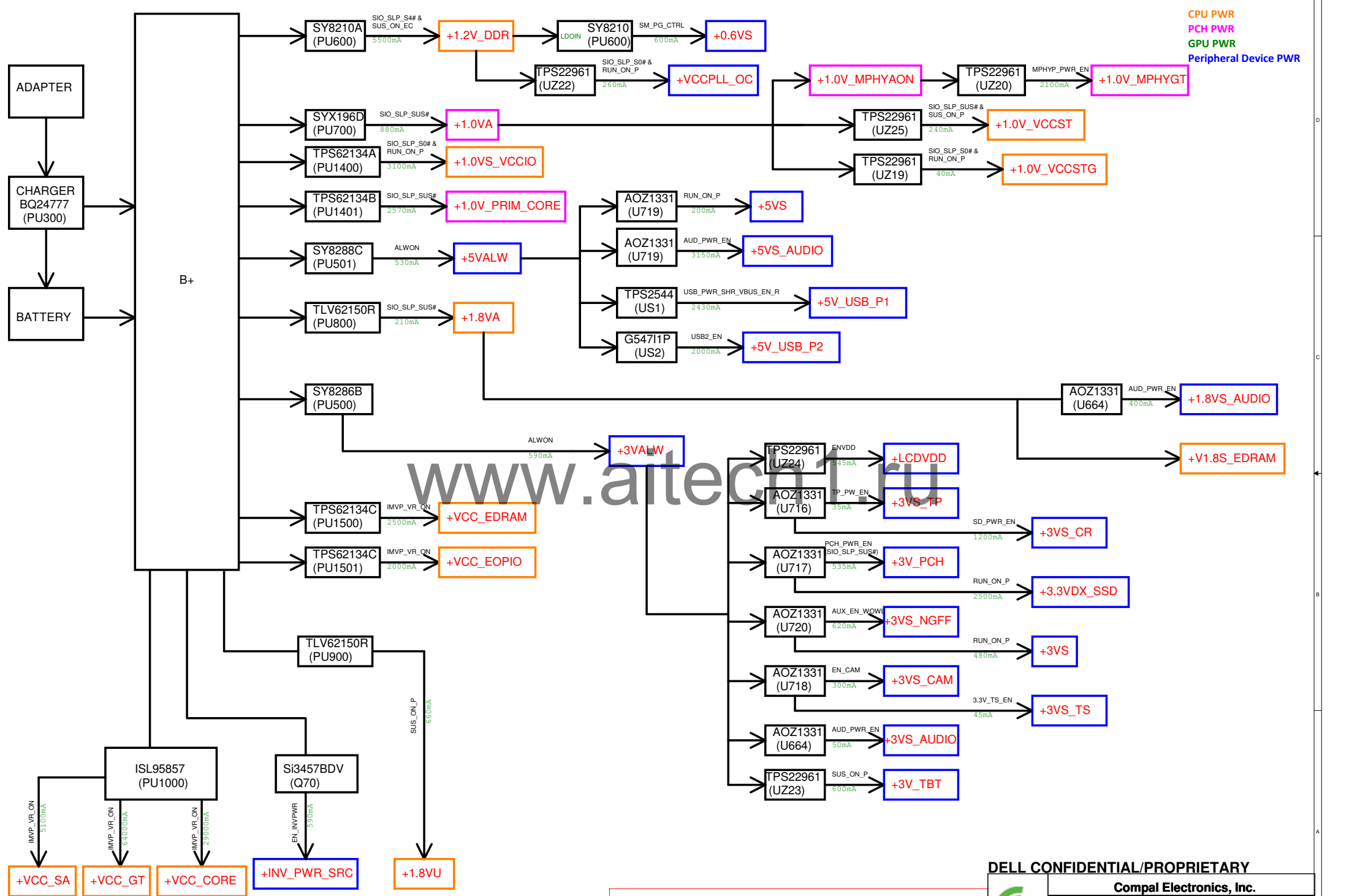
CLK	DIFFERENTIAL CLK#	DESTINATION	PCI EXPRESS PORT#	DESTINATION
	CLKOUT_PCIE0	Alpine Ridge	Lane 1	Alpine Ridge
	CLKOUT_PCIE1	NGFF CARD WLAN	Lane 2	Alpine Ridge
	CLKOUT_PCIE2		Lane 3	
	CLKOUT_PCIE3	M.2 SSD / PCIe	Lane 4	
	CLKOUT_PCIE4		Lane 5	NGFF CARD WLAN
	CLKOUT_PCIE5	Card Reader	Lane 6	Card Reader
	FLEX CLK#	DESTINATION	Lane 7	
	CLKOUT_LPC_0	EC LPC	Lane 8	
	CLKOUT_LPC_1	Debug	Lane 9	M.2 SSD
			Lane 10	M.2 SSD
			Lane 11	M.2 SSD
			Lane 12 / SATA 2	M.2 SSD

SATA PORT#	DESTINATION
SATA-0	
SATA-1A	
SATA-1B	
SATA-2	M.2 SSD

Symbol Note :

 : means Digital Ground

 : means Analog Ground



CPU PWR
PCH PWR
GPU PWR
Peripheral Device PWR

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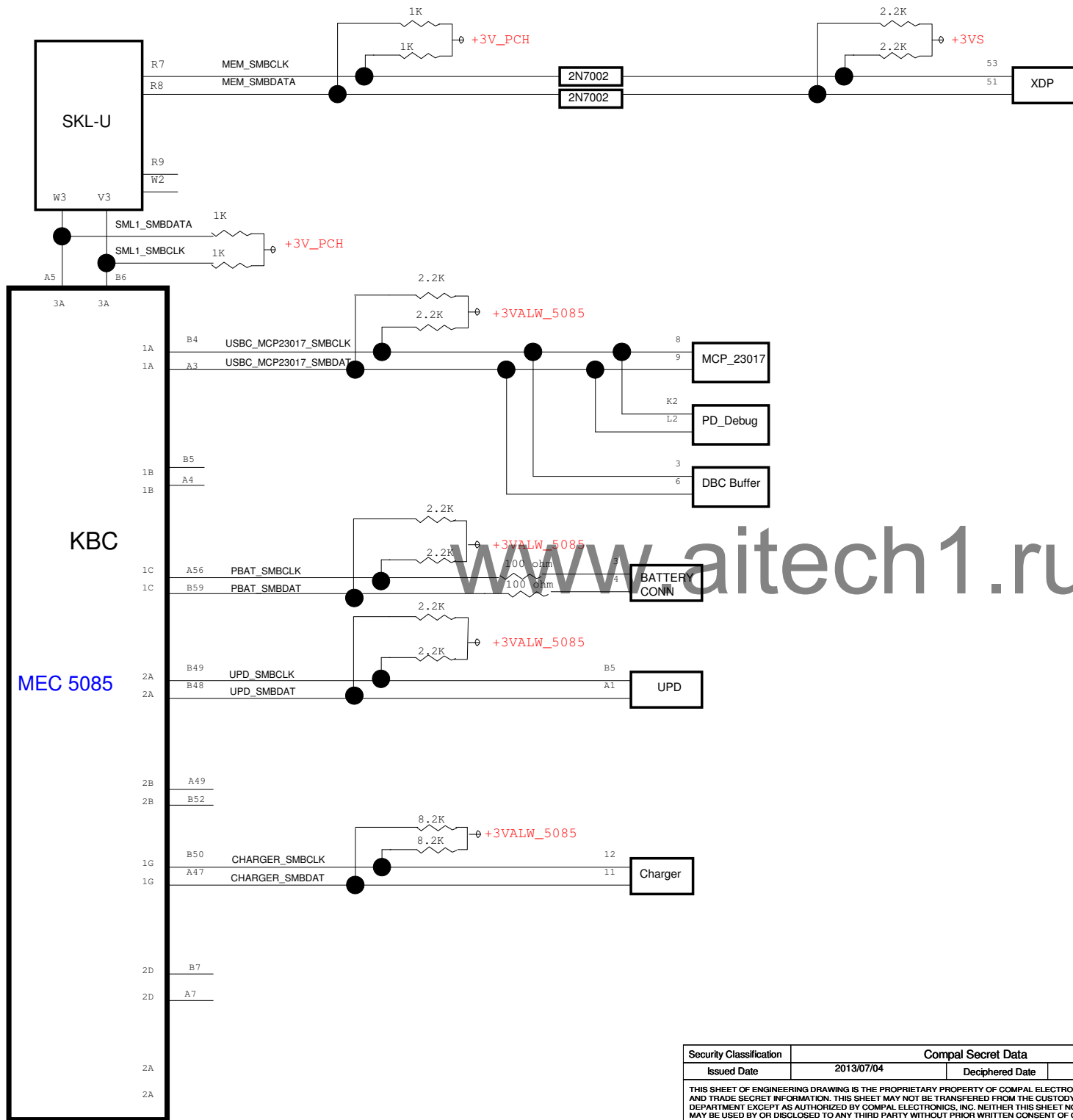
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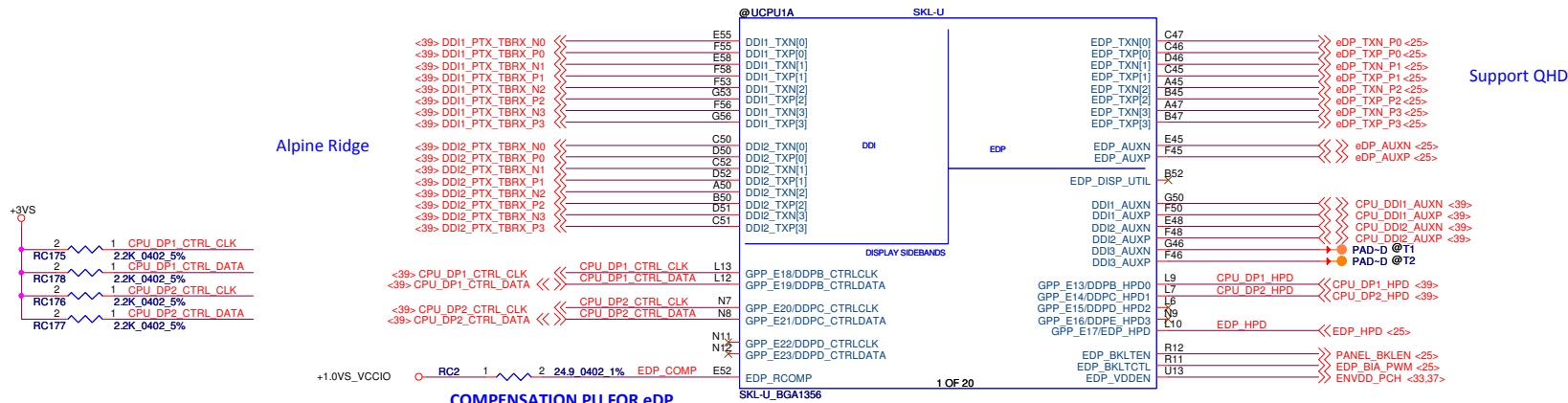
Compal Electronics, Inc.

P05-Power rails

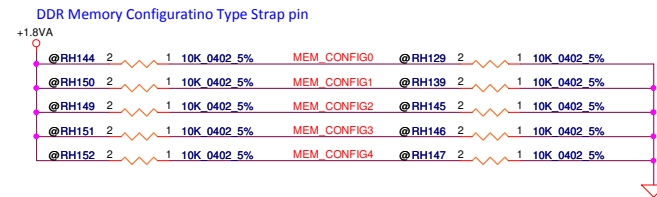
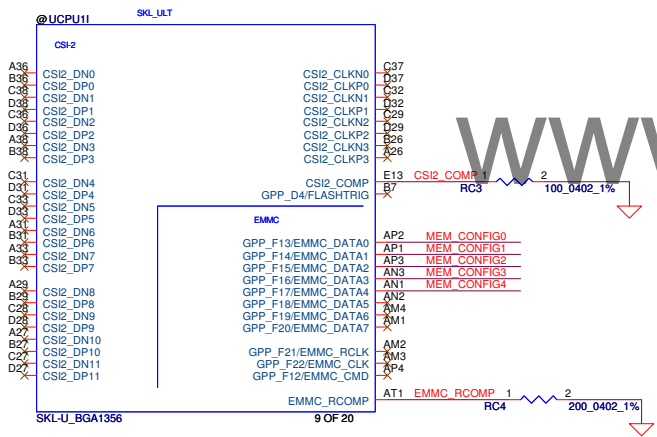
LA-C881P

Title	P05-Power rails		
Size	Document Number	Rev	
Date	Tuesday, October 13, 2015	Sheet	5 of 59





CAD Note: Trace width=20 mils, Isolation Spacing=25mil, Max length=100 mils.

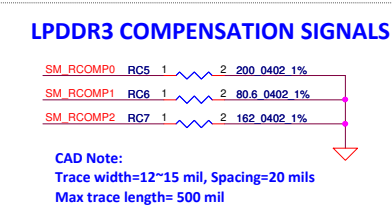


GPIO Pin	Pin Name	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	0	1	0	1	0	1	0	1	0
GPP_D6	MEM_CONFIG1	0	0	1	1	0	0	1	1	0
GPP_D7	MEM_CONFIG2	0	0	0	0	1	1	1	1	0
GPP_D8	MEM_CONFIG3	0	0	0	0	0	0	0	0	1
GPP_D9	MEM_CONFIG4	0	0	0	0	0	0	0	0	0

GPIO Pin	Pin Name	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	1	0	1	0	1	0	1	0	1
GPP_D6	MEM_CONFIG1	0	1	1	0	0	1	1	0	0
GPP_D7	MEM_CONFIG2	0	0	0	1	1	1	1	0	0
GPP_D8	MEM_CONFIG3	1	1	1	1	1	1	1	0	0
GPP_D9	MEM_CONFIG4	0	0	0	0	0	0	0	1	1

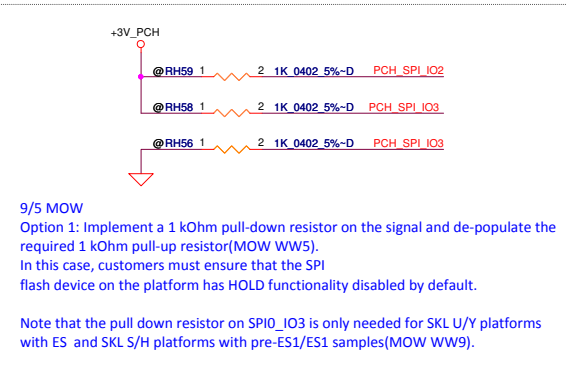
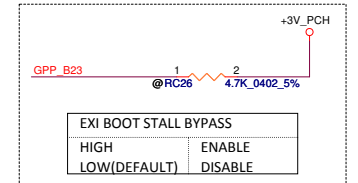
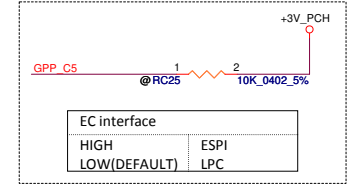
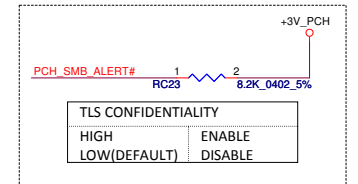
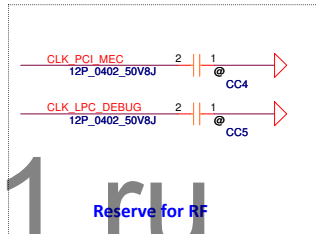
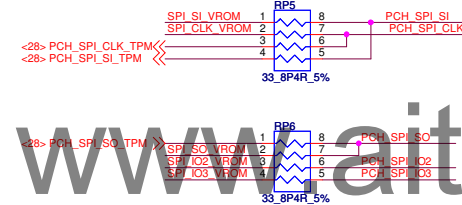
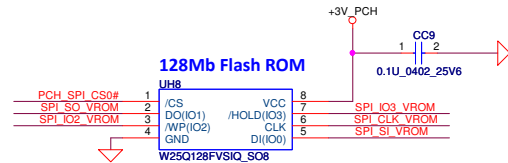
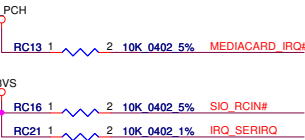
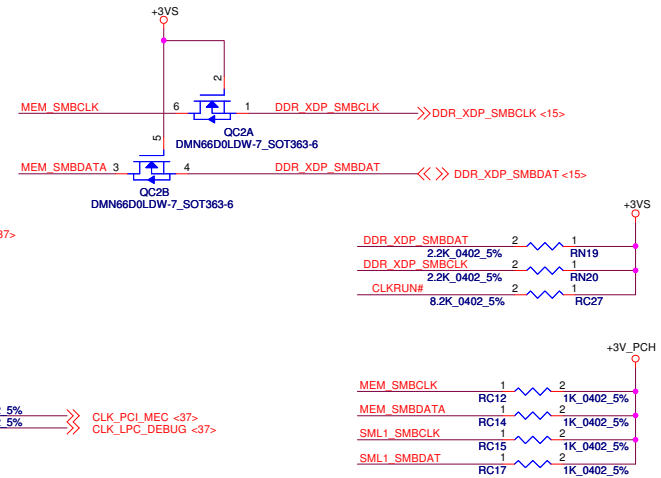
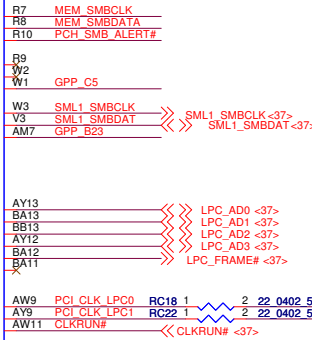
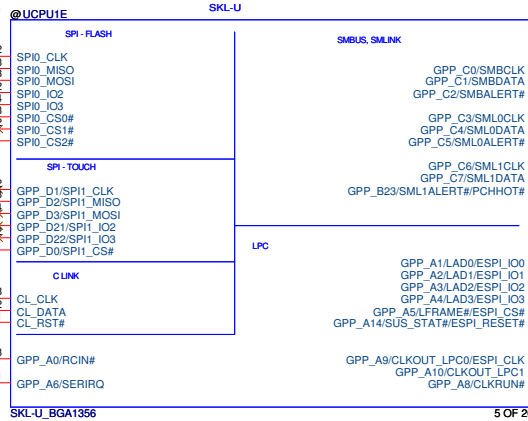
GPIO Pin	Pin Name	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	0	1	0	1	0	1	0	1	0
GPP_D6	MEM_CONFIG1	1	1	0	0	1	1	0	0	1
GPP_D7	MEM_CONFIG2	0	0	1	1	1	1	0	0	0
GPP_D8	MEM_CONFIG3	0	0	0	0	0	0	1	1	1
GPP_D9	MEM_CONFIG4	1	1	1	1	1	1	1	1	1

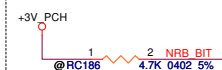
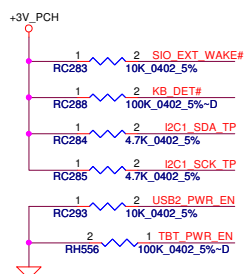
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Issued Date	2013/07/04	Deciphered Date	2013/10/28
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Issued Date	2013/07/04	Deciphered Date	2013/10/28	Title	P08-MCP(2/14)LPDDR3		
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					LA-C881P		1.0
				Date:	Tuesday, October 13, 2015		Sheet

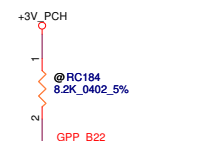
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 SPI_MISO= SPI_IO1
 PCH EDS R0.7 p.235~236



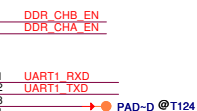
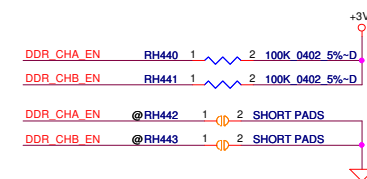
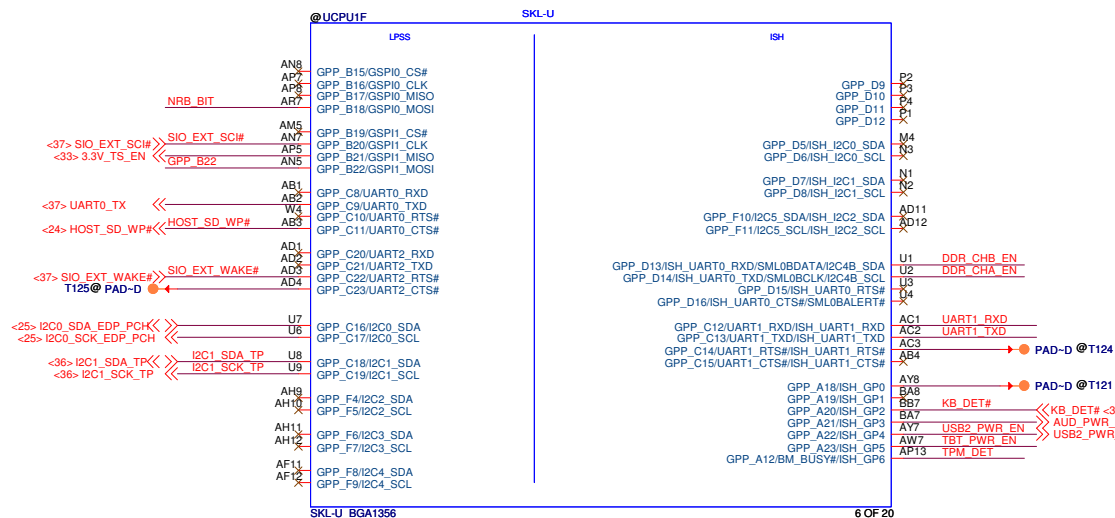


NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE

Weak IPD

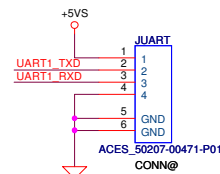


BOOT BIOS Destination(Bit 6)	
HIGH	LPC
LOW(DEFAULT)	SPI



TPM BOM Optional

TPM_DET	
TPM	1 = W/TPM 0 = W/O TPM



M.2 SSD
PCIe Gen3 x4

SATA SSD

WLAN
PCIe Gen2 x1

Cardreader
PCIe Gen2 x1

Alpine Ridge
PCIe Gen3 x2

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<30> SATA_PTX_SSDRX_P2>>

@UCPU1H

SKL-U

PCIE/USB3/SATA
H13 PCIE1_RXN/USB3_5_RXN
G13 PCIE1_RXP/USB3_5_RXP
B17 PCIE1_TXN/USB3_5_TXN
A17 PCIE1_TXP/USB3_5_TXP

G11 PCIE2_RXN/USB3_6_RXN
E11 PCIE2_RXP/USB3_6_RXP
D19 PCIE2_TXN/USB3_6_TXN
C16 PCIE2_TXP/USB3_6_TXP

H18 PCIE3_RXN
C18 PCIE3_RXP
D17 PCIE3_TXN
C17 PCIE3_TXP

G15 PCIE4_RXN
B15 PCIE4_RXP
B19 PCIE4_TXN
A19 PCIE4_TXP

F16 PCIE5_RXN
E16 PCIE5_RXP
C19 PCIE5_TXN
D19 PCIE5_TXP

G18 PCIE6_RXN
F18 PCIE6_RXP
D20 PCIE6_TXN
C20 PCIE6_TXP

F20 PCIE7_RXN/SATA0_RXN
E20 PCIE7_RXP/SATA0_RXP
B21 PCIE7_TXN/SATA0_TXN
A21 PCIE7_TXP/SATA0_TXP

G21 PCIE8_RXN/SATA1A_RXN
F21 PCIE8_RXP/SATA1A_RXP
D21 PCIE8_TXN/SATA1A_TXN
C21 PCIE8_TXP/SATA1A_TXP

E22 PCIE9_RXN
E23 PCIE9_RXP
B23 PCIE9_TXN
A23 PCIE9_TXP

F25 PCIE10_RXN
E25 PCIE10_RXP
D23 PCIE10_TXN
C23 PCIE10_TXP

F9 PCIE11_RXN/SATA1B_RXN
E9 PCIE11_RXP/SATA1B_RXP
D24 PCIE11_TXN/SATA1B_TXN
C24 PCIE11_TXP/SATA1B_TXP

E30 PCIE12_RXN/SATA2_RXN
D25 PCIE12_RXP/SATA2_RXP
B25 PCIE12_TXN/SATA2_TXN
A25 PCIE12_TXP/SATA2_TXP

SKL-U_BGA1356

SSIC/USB3

USB3_1_RXN
USB3_1_RXP
USB3_1_TXN
USB3_1_TXP

USB3_2_RXN/SSIC_1_RXN
USB3_2_RXP/SSIC_1_RXP
USB3_2_TXN/SSIC_1_TXN
USB3_2_TXP/SSIC_1_TXP

USB3_3_RXN/SSIC_2_RXN
USB3_3_RXP/SSIC_2_RXP
USB3_3_TXN/SSIC_2_TXN
USB3_3_TXP/SSIC_2_TXP

USB3_4_RXN
USB3_4_RXP
USB3_4_TXN
USB3_4_TXP

USB2N_1
USB2P_1

USB2N_2
USB2P_2

USB2N_3
USB2P_3

USB2N_4
USB2P_4

USB2N_5
USB2P_5

USB2N_6
USB2P_6

USB2N_7
USB2P_7

USB2N_8
USB2P_8

USB2N_9
USB2P_9

USB2N_10
USB2P_10

USB2_COMP
USB2_ID
USB2_VBUSSENSE

GPP_E0/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#

GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2

GPP_E0/SATA0PCIE0/SATAGP0
GPP_E1/SATA0PCIE1/SATAGP1
GPP_E2/SATA0PCIE2/SATAGP2

GPP_E8/SATA0LED#

RC44 1 2 113 0402 1%
RC19 1 2 0.0402 1%
RC20 1 2 1K 0402 5%

TBT_USB_OC0#
USB_OC1#
USB_OC2#
USB_OC3#

TBT_USB_OC0#<41>
USB_OC1#<24>
USB_OC2#<31>

SSD_DEVSLP<30>
SSD_IFDET<30>

R07_0720: Add GPIO to disable SATA#1

8 OF 20

H8 USB3RN1<24>
G8 USB3RP1<24>
D13 USB3TN1<24>
D13 USB3TP1<24>

J6 USB3RN2<31>
H6 USB3RP2<31>
B13 USB3TN2<31>
A13 USB3TP2<31>

J10 USB3RN3<31>
H10 USB3RP3<31>
B15 USB3TN3<31>
A15 USB3TP3<31>

E10 USB3RN4<25>
H10 USB3RP4<25>
B15 USB3TN4<25>
A15 USB3TP4<25>

AB9 USB2N_1<24>
AB10 USB2P_1<24>

AD6 USB2N_2<31>
AD7 USB2P_2<31>

AH3 USB2N_3<29>
AJ3 USB2P_3<29>

AD9 USB2N_4<25>
AD10 USB2P_4<25>

AJ1 USB2N_5<25>
AJ2 USB2P_5<25>

AF6 USB2N_6<25>
AF7 USB2P_6<25>

AH1 USB2N_7<25>
AH2 USB2P_7<25>

AF8 USB2N_8<25>
AF9 USB2P_8<25>

AG1 USB2N_9<25>
AG2 USB2P_9<25>

AH7 USB2N_10<25>
AH8 USB2P_10<25>

RC44 1 2 113 0402 1%
RC19 1 2 0.0402 1%
RC20 1 2 1K 0402 5%

TBT_USB_OC0#
USB_OC1#
USB_OC2#
USB_OC3#

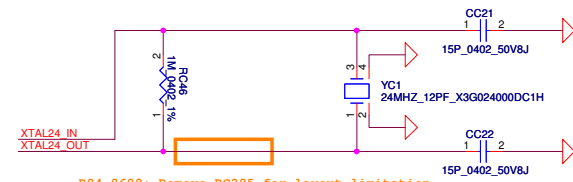
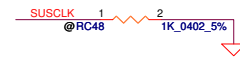
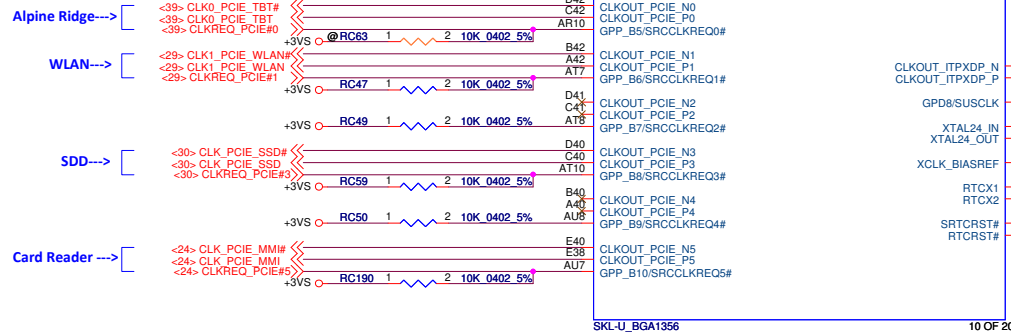
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USB_OC1#<24>
USB_OC2#<31>

SSD_DEVSLP<30>
SSD_IFDET<30>

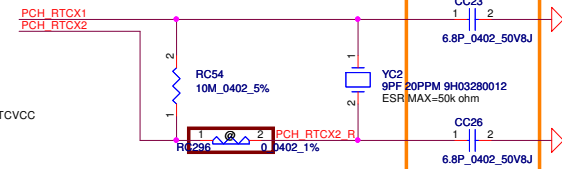
R07_0720: Add GPIO to disable SATA#1

8 OF 20

+3V_PCH
TBT_USB_OC0# 1 2 10K_0402_5%
USB_OC1# RC189 1 2 10K_0402_5%
USB_OC2# RC185 1 2 10K_0402_5%
USB_OC3# RC188 1 2 10K_0402_5%
RC191 1 2 10K_0402_5%

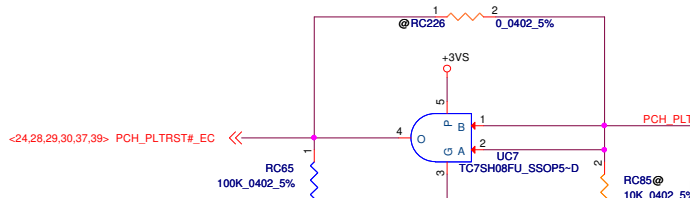
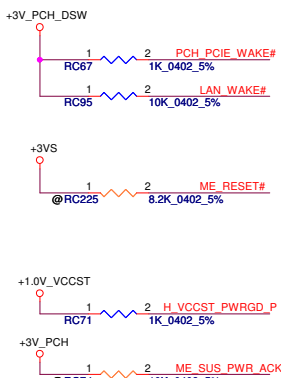


R04_0609: Remove RC295 for layout limitation



R04_0609: Fine tune cap by vendor suggestion

CMOS1 must take care short & touch risk on layout placement

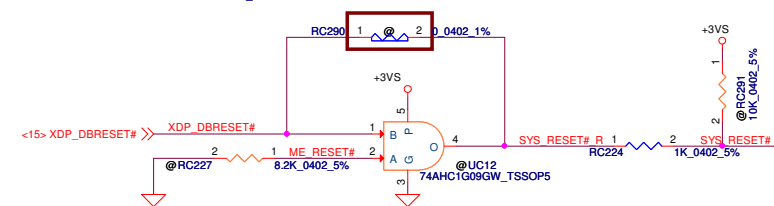
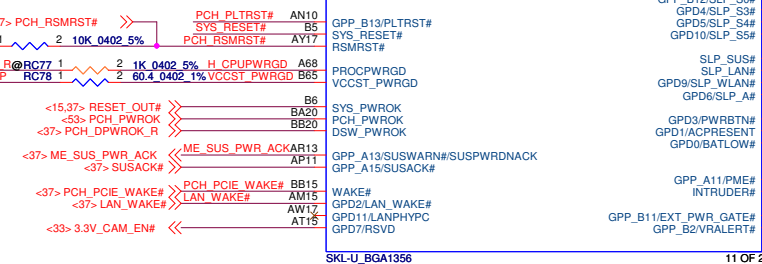
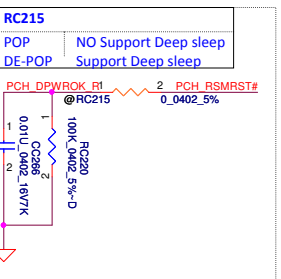
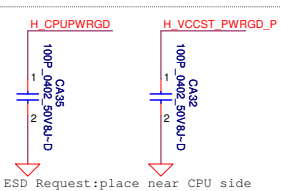


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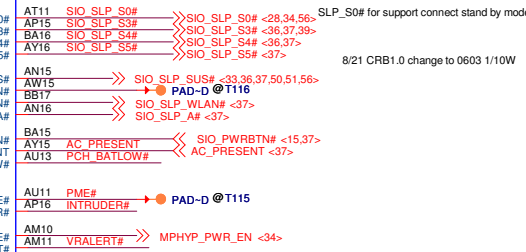


SLP_S0# for support connect stand by mode

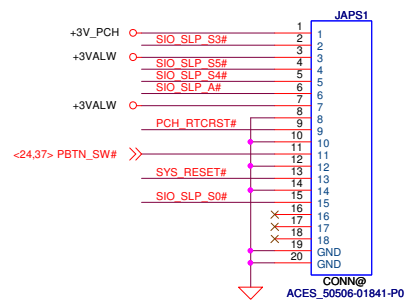
8/21 CRB1.0 change to 0603 1/10W



if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)



APS CONN



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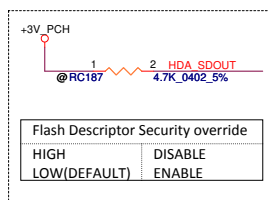
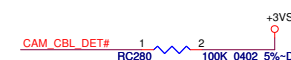
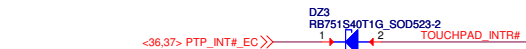
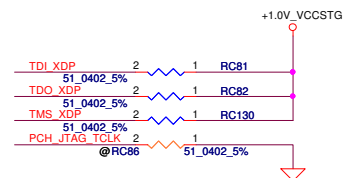
Document Number

LA-C881P

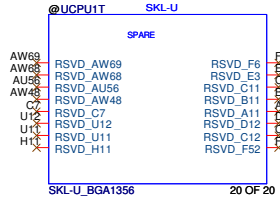
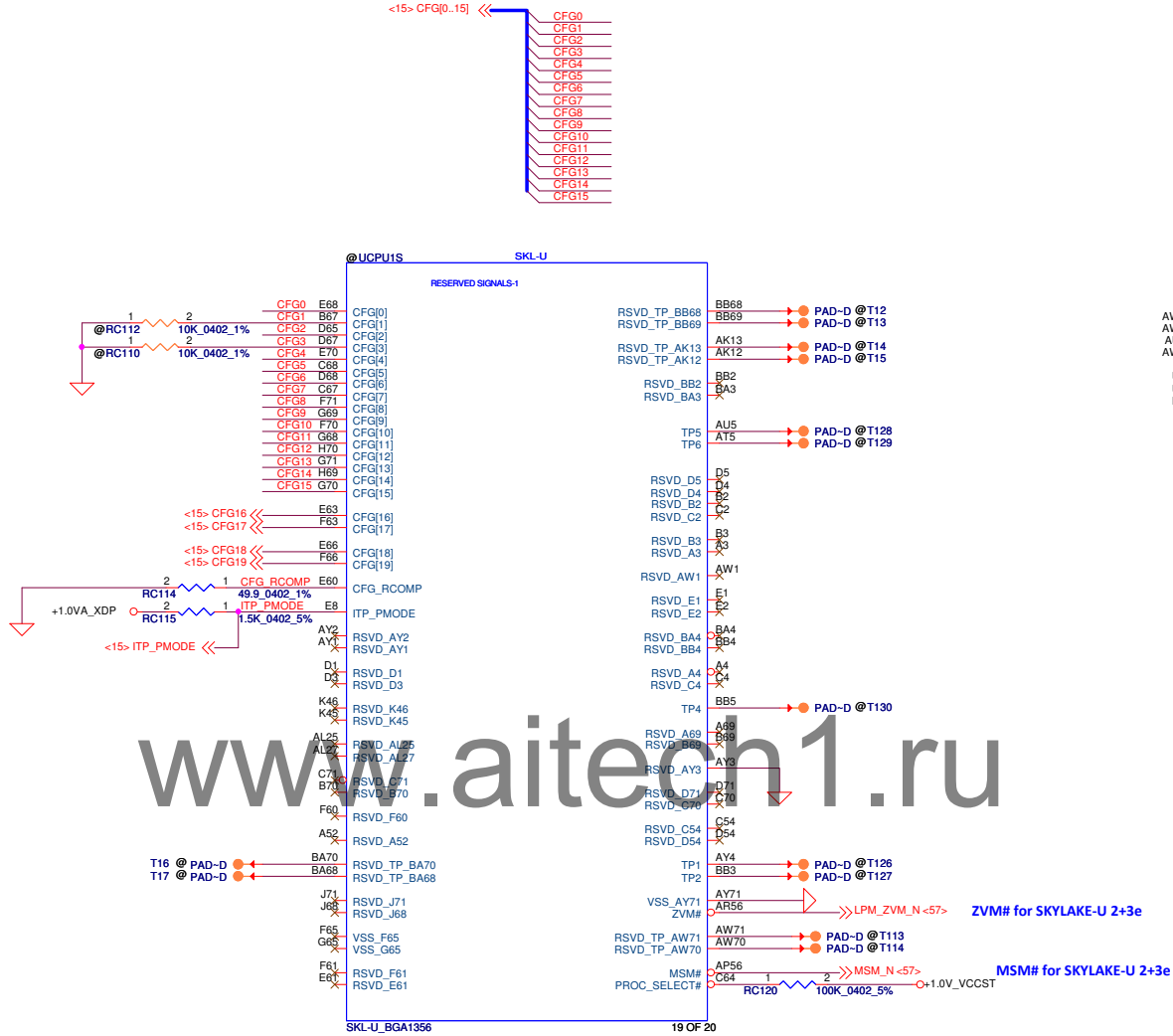
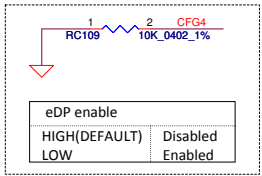
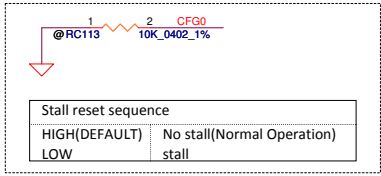
Date: Tuesday, October 13, 2015

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Issued Date	2013/07/04	Deciphered Date	2013/10/28
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P12-MCP(6/14)CLK,PM,RTC			Rev 1.0



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Issued Date	2013/07/04	Deciphered Date	2013/10/28	P13-MCP(7/14)MISC, JTAG, HDA, SDIO
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Date:	Tuesday, October 13, 2015	Sheet	13 of 59	Rev 1.0



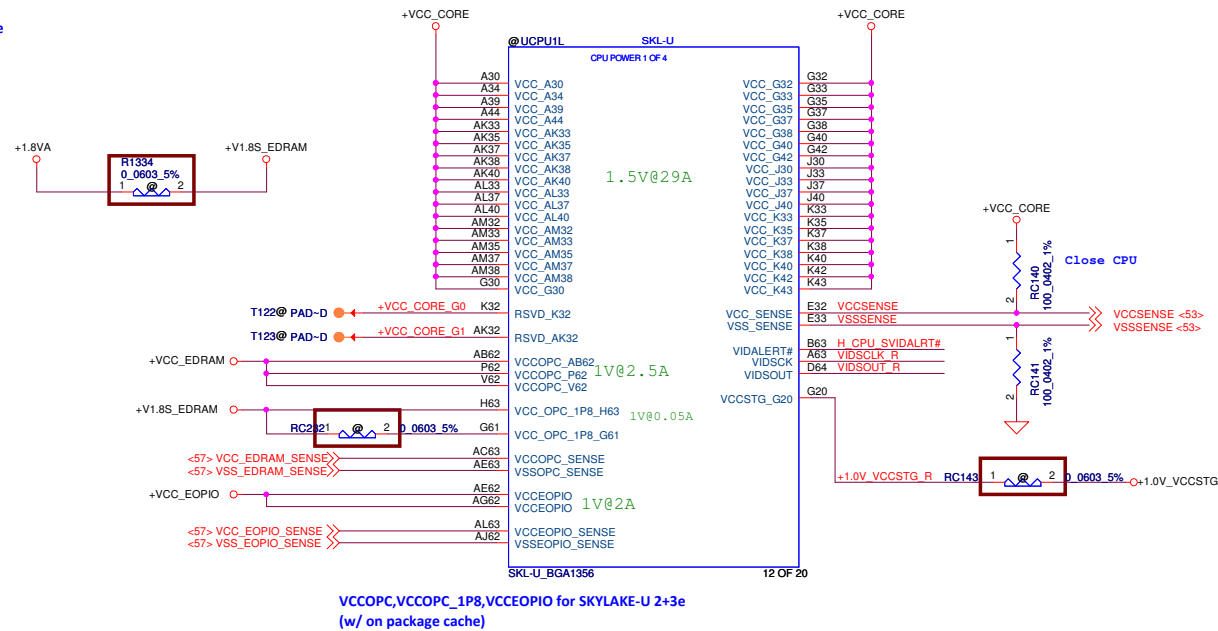
Security Classification	Compal Secret Data	
Issued Date	2013/07/04	Deciphered Date 2013/10/28
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Title	P14-MCP(8/14)CFG,RSVD
Document Number	LA-C881P
Date: Tuesday, October 13, 2015	Rev 1.0
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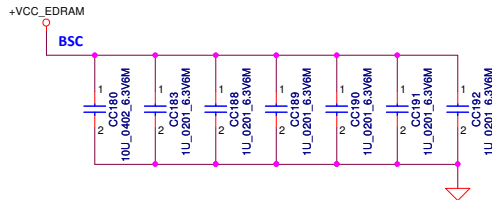
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

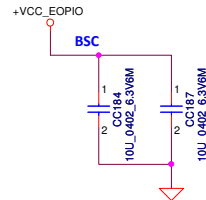
+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A
+V1.8S_EDRAM: 1.8V, 50mA
+VCC_EOPIO: 0.8~1V, 2A



+VCC_EDRAM Decoupling Requirement
Back Side (underneath the package) :
10U_0402*1 pcs + 1U_0201*6 pcs



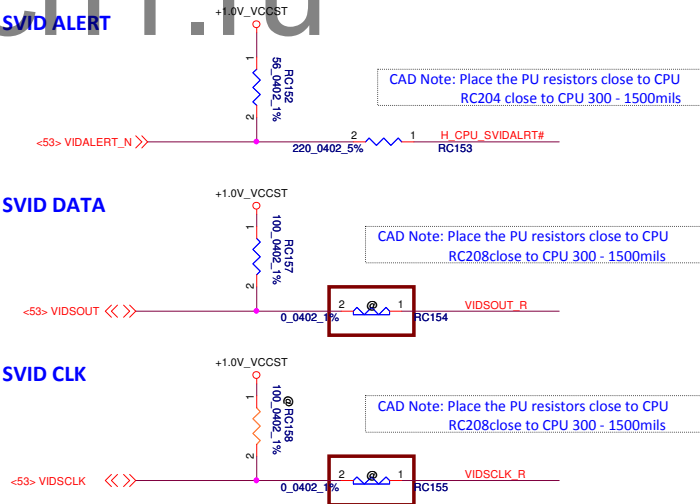
+VCC_EOPIO Decoupling Requirement
Back Side (underneath the package) :
10U_0402*2 pcs



SVID ALERT

SVID DATA

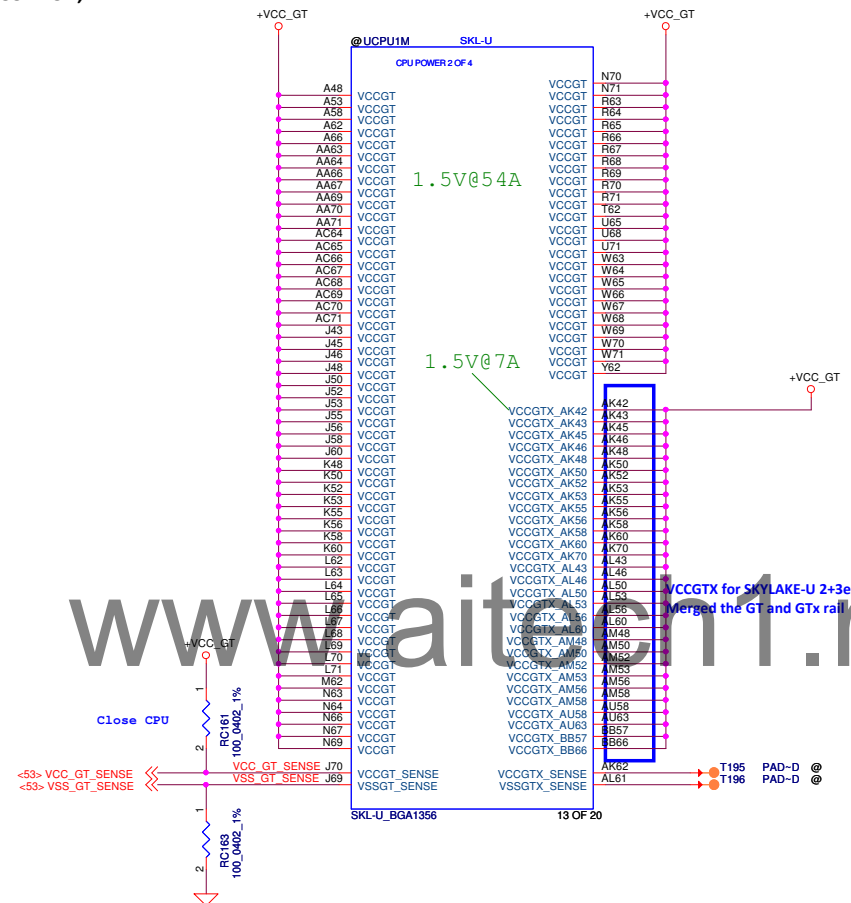
SVID CLK



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Date: Tuesday, October 13, 2015			Rev 1.0
Sheet 16 of 59			

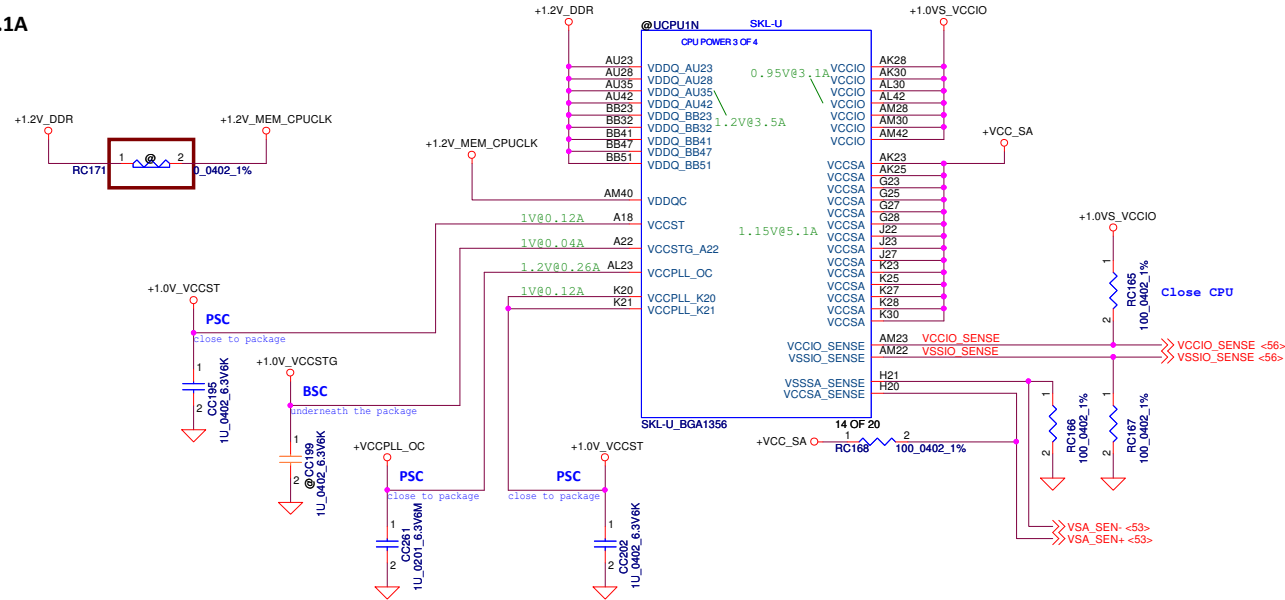
+VCCGT: 0.55~1.5V, 54A
+VCCGTX : 0.55~1.5V, 7A



Genomic map of the VCCGTX gene region on chromosome 1. The map shows the VCCGTX gene structure with exons and introns. A red circle highlights the VCCGTX GT (GT) region. The map is flanked by the VCCGTX GT (GT) region on the left and the VCCGTX GT (GT) region on the right. The map is labeled with 'VCCGTX GT (GT)' and 'VCCGTX GT (GT)'.

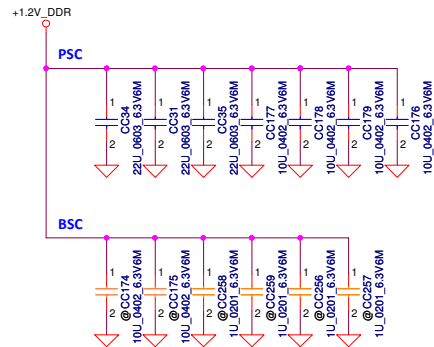
Security Classification	Compal Secret Data			<div style="text-align: right;"> DECLASSIFIED CONFIDENTIAL CONFIDENTIAL </div>	
Issued Date	2013/07/04	Deciphered Date	2013/10/28	Title P17-MCP(11/14)PWR-VCCGT	
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+1.2V_DDR: 1.2V, 3.5A
 +1.0V_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA
 +1.0V_VCCSTG: 1V, 40mA
 +VCCPLL_OC: 1.2V, 260mA
 +1.0VS_VCCIO: 0.85~0.95V, 3.1A
 +VCC_SA: 1.15V, 5.1A

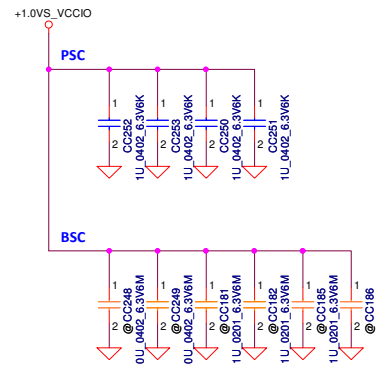


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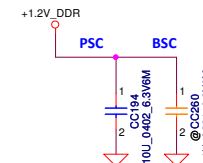
+1.2_DDR Decoupling Requirement
 Back Side (underneath the package):
 10U_0402*2 pcs + 10_0201*4 pcs (8)
 Primary Side (close to package):
 10U_0402*4 pcs + 22U_0603*3 pcs



+1.0VS_VCCIO Decoupling Requirement
 Back Side (underneath the package):
 10U_0402*2 pcs + 10_0201*4 pcs (8)
 Primary Side (close to package):
 10U_0402*4 pcs



+1.2V_MEM_CPUCLK (VDDQC) Place on CPU
 Back Side (underneath the package):
 10_0201*1 pcs (8)
 Primary Side (close to package):
 10U_0402 * 1 pcs



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P18-MCP(12/14)PWR-VCCIO.MEM

LA-C881P

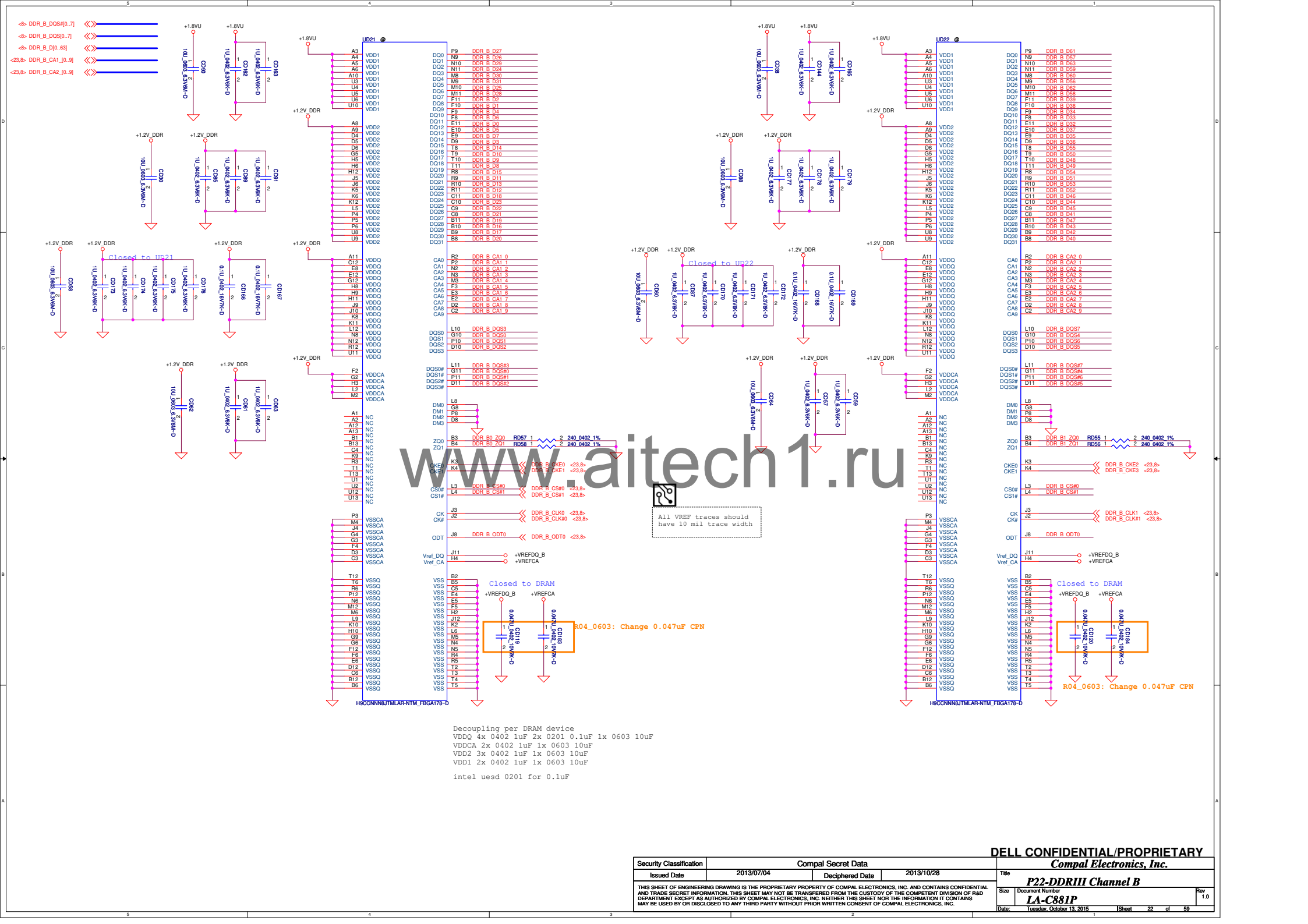
Document Number: LA-C881P, Date: Tuesday, October 13, 2015, Sheet: 18 of 59

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



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Issued Date	2013/07/04	Deciphered Date	2013/10/28	Title	P20-MCP(14/14)VSS Document Number LA-C88IP
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Date:				Tuesday, October 13, 2015	Sheet 20 of 59



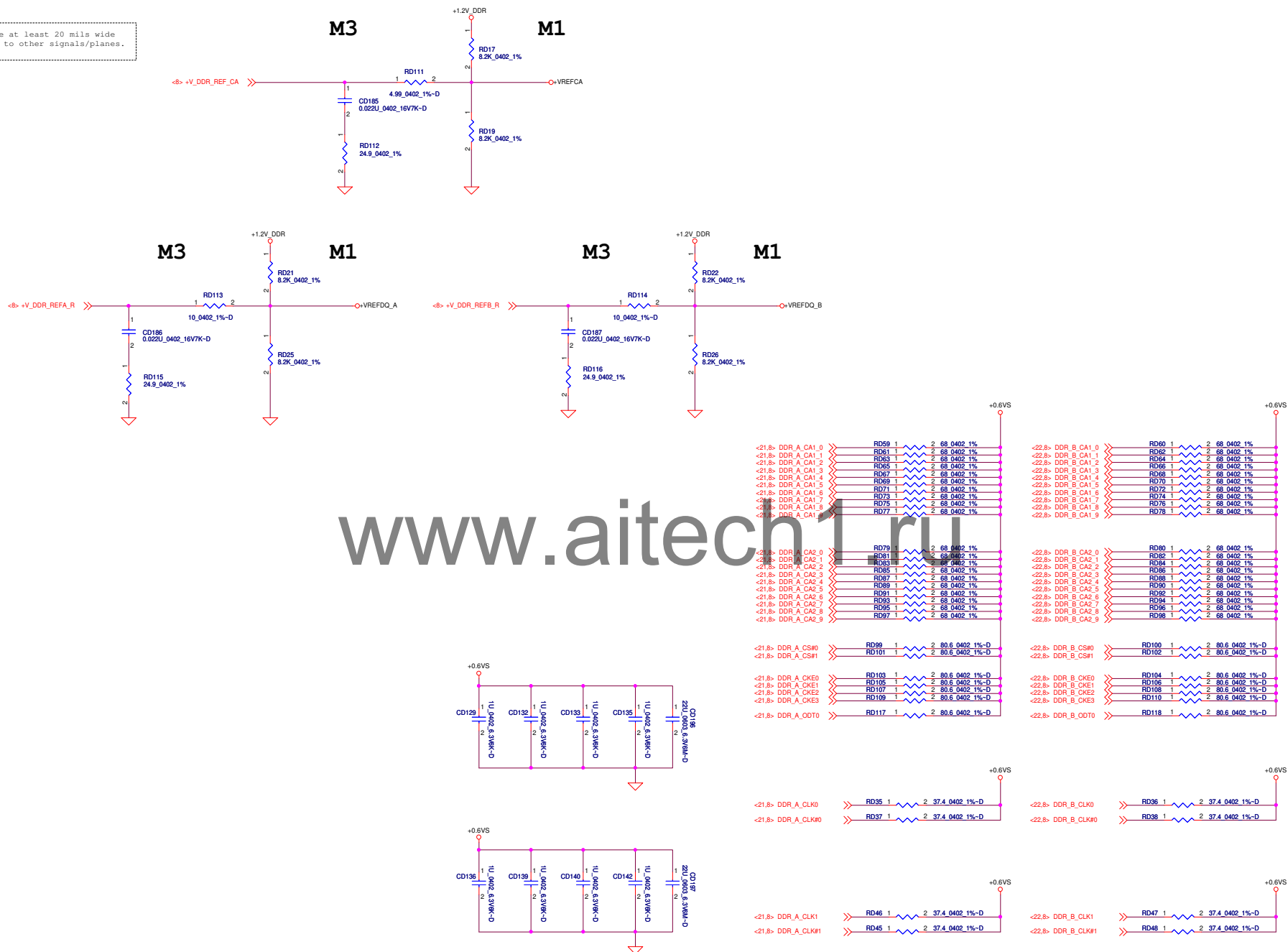
Decoupling per DRAM device
VDDQ 4x 0402 1uF 2x 0201 0.1uF 1x 0603 10uF
VDDCA 2x 0402 1uF 1x 0603 10uF
VDD2 3x 0402 1uF 1x 0603 10uF
VDD1 2x 0402 1uF 1x 0603 10uF

intel uesd 0201 for 0.1uF

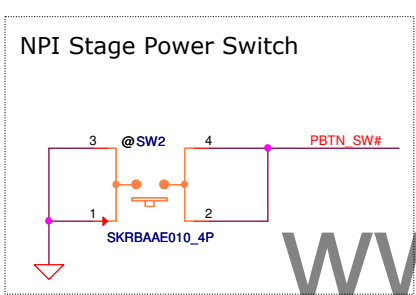
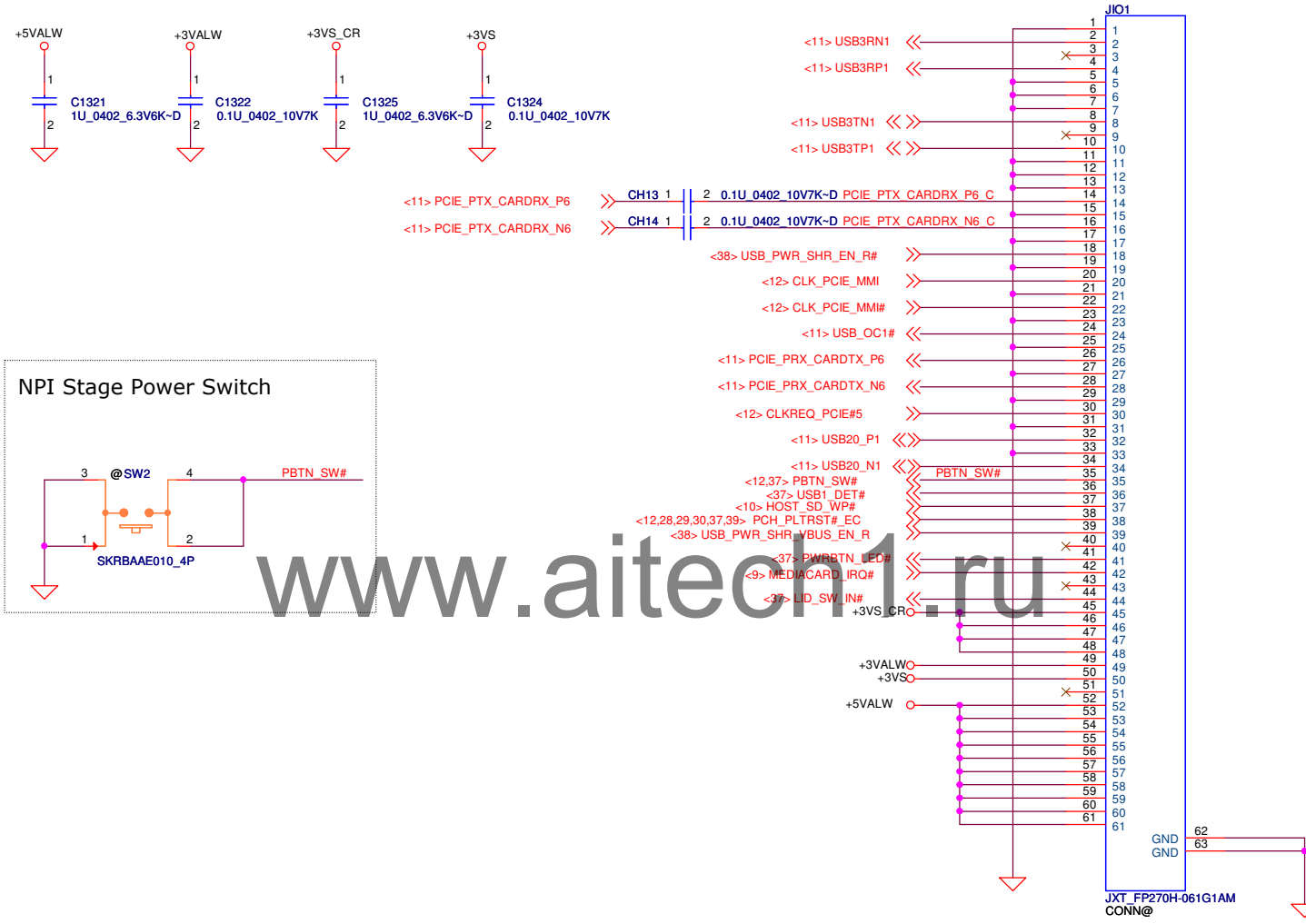
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Issued Date		Deciphered Date		P22-DDRIII Channel B	
2013/07/04		2013/10/28		Document Number	
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VREF traces should be at least 20 mils wide
with 20 mils spacing to other signals/planes.



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Issued Date				2013/07/04	Deciphered Date	2013/10/28	Document Number
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				Tuesday, October 13, 2015		Sheet 23 of 59	

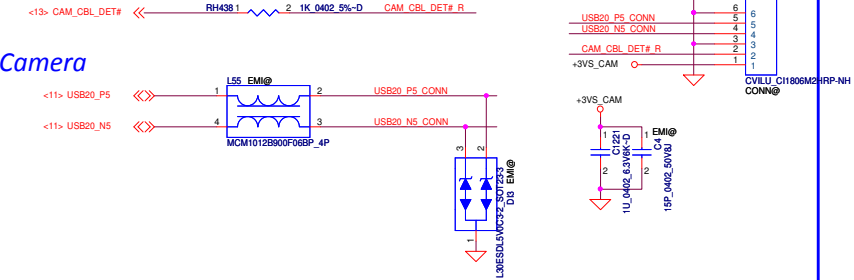


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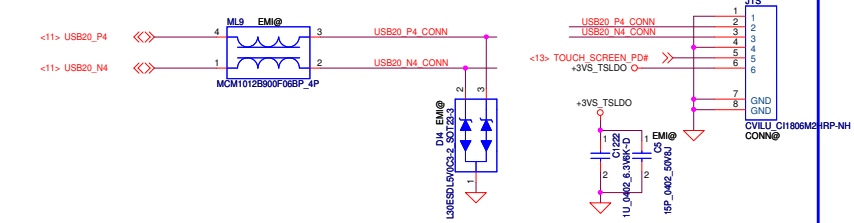
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Issued Date	2013/07/04	Deciphered Date	2013/10/28	P24-BTB CONN	
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				LA-C881P	Rev 1.0
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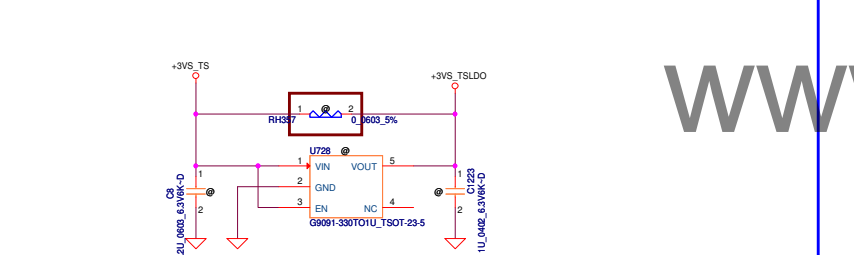
Camera + Touch Screen



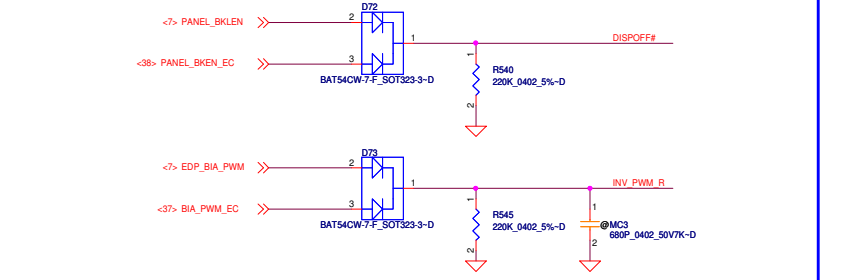
Touch Screen



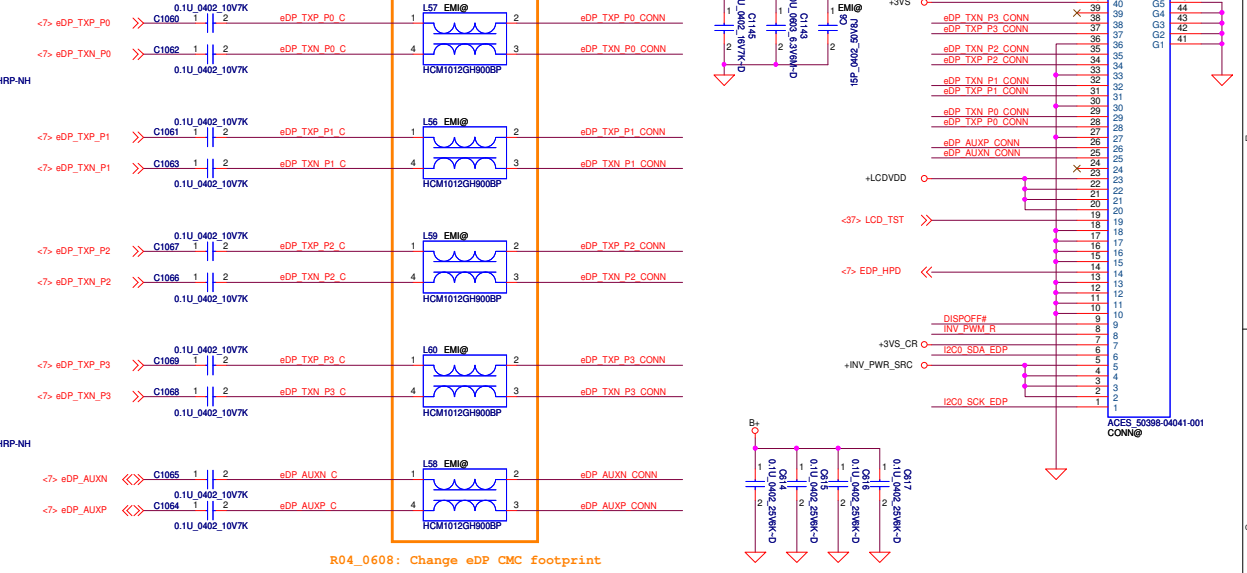
Touch Screen LDO



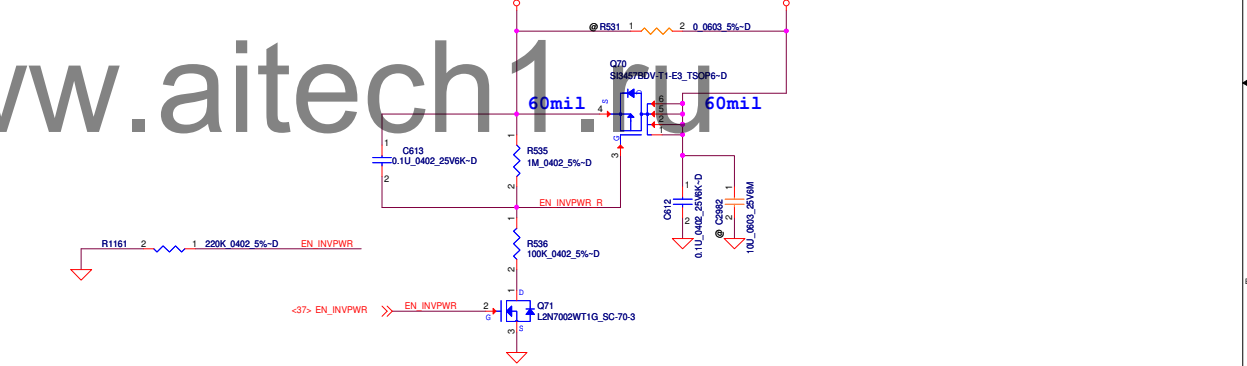
BackLight PWM Control



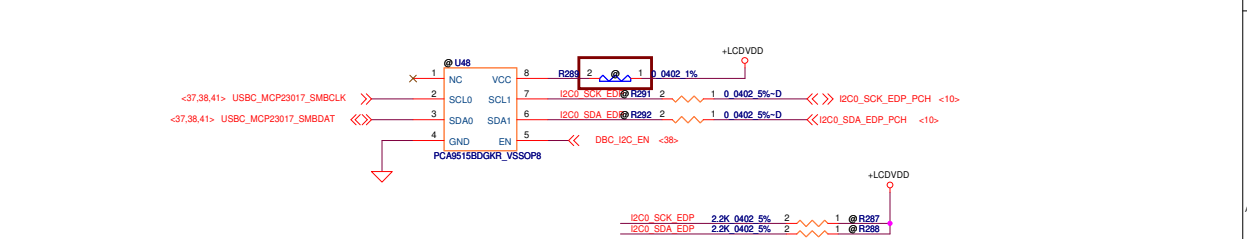
eDP Conn



eDP BackLight Power

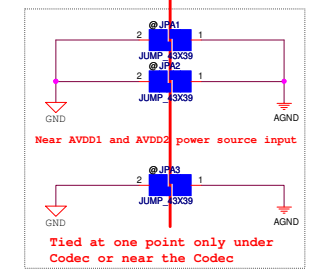
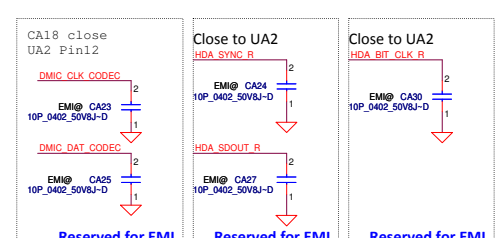
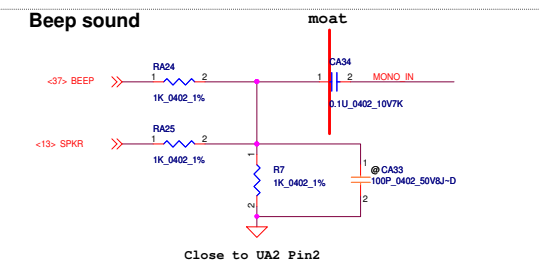
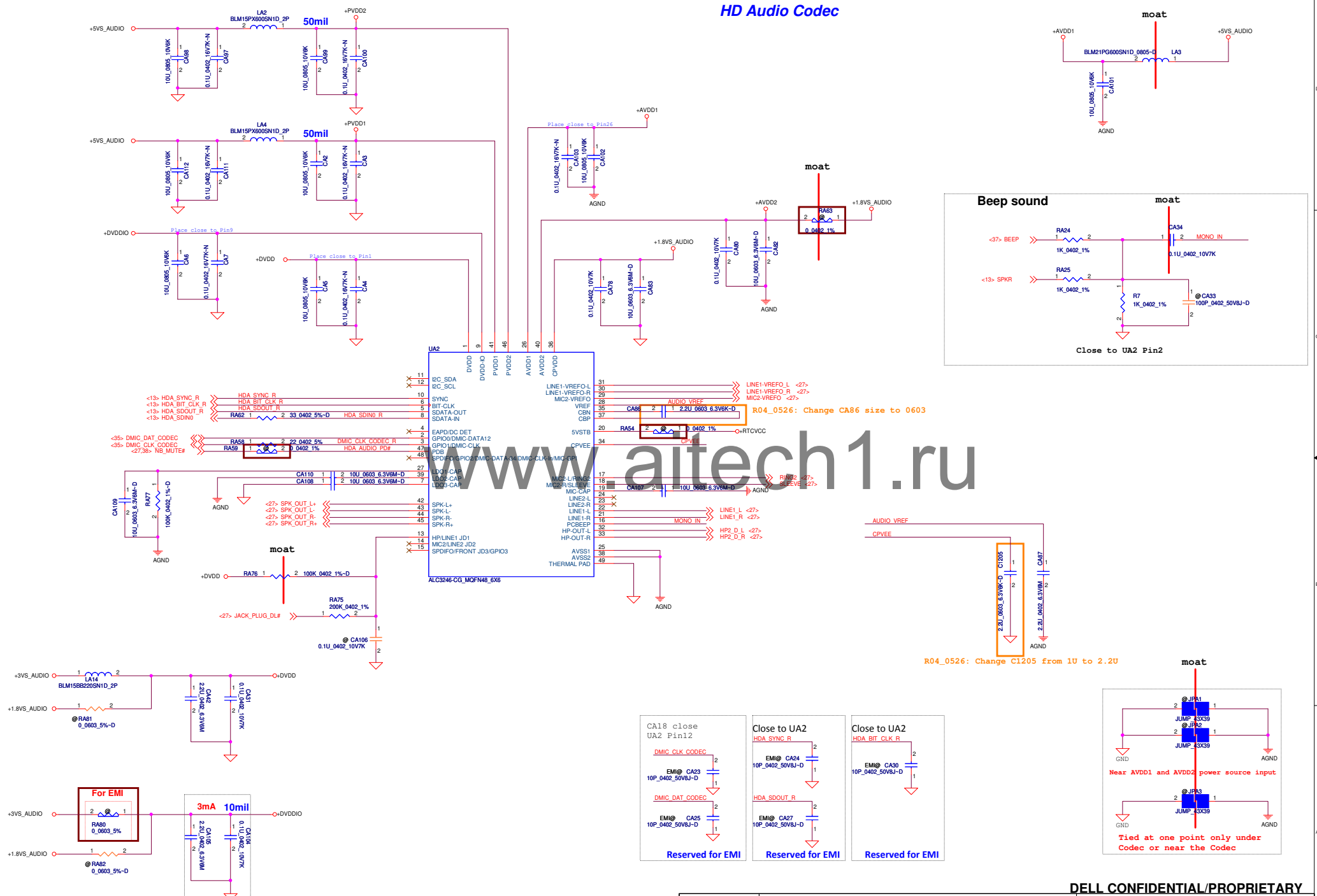


DBC delay schematic



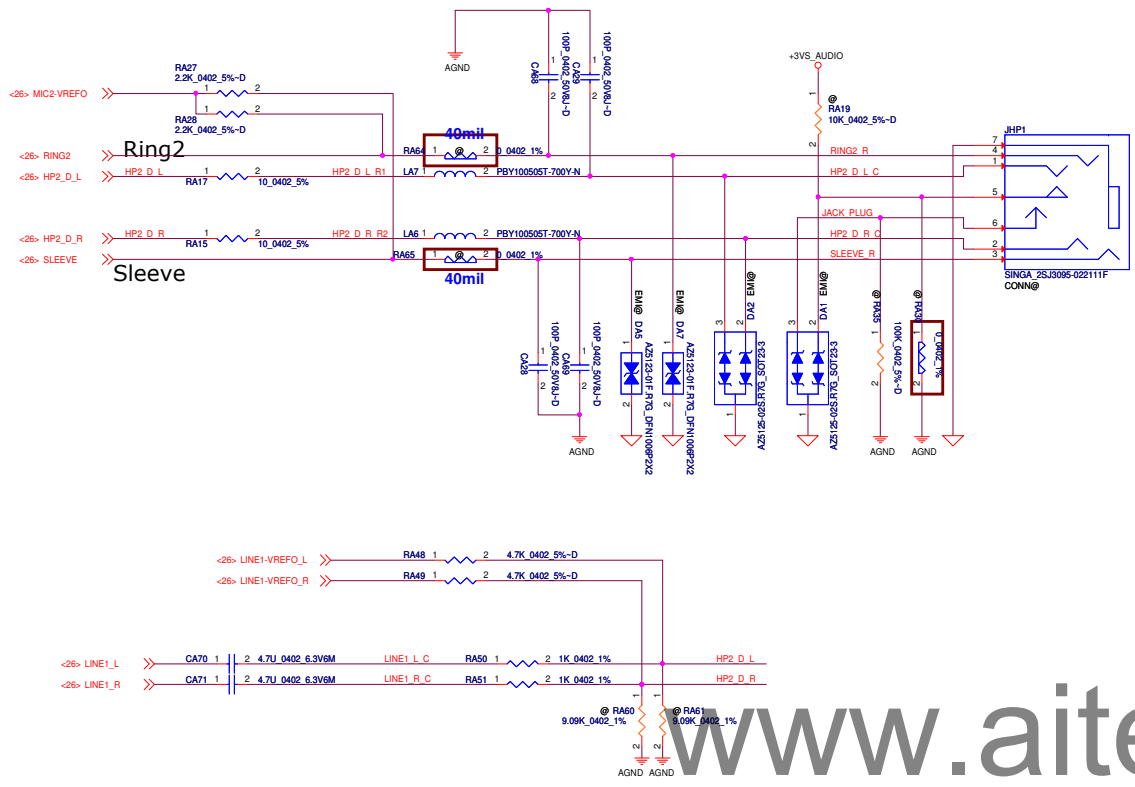
Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
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2013/07/04		2013/10/28		P25-eDP/ Camera CONN	
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				LA-C881P	
				Rev 1.0	
				Date: Tuesday, October 13, 2015	
				Sheet 25 of 59	

HD Audio Codec

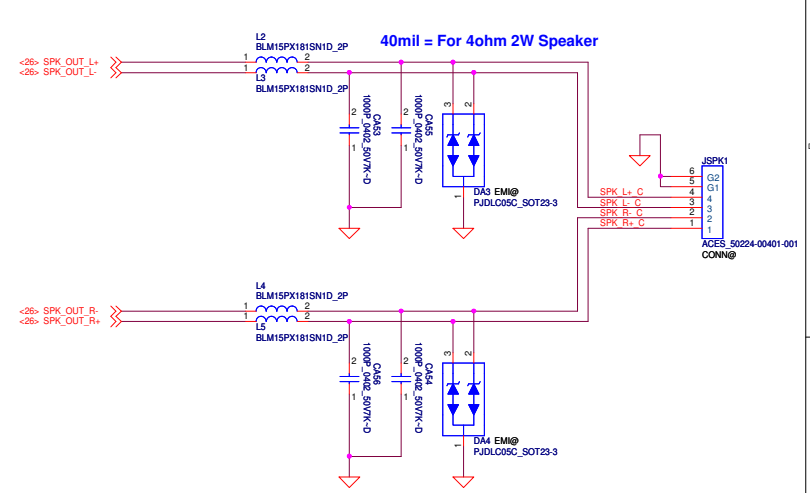


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Issued Date		Deciphered Date		P26-Audio Codec	
2013/07/04		2013/10/28		Document Number	
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Date		Tuesday, October 13, 2015		Sheet 26 of 59	

Universal Audio Jack

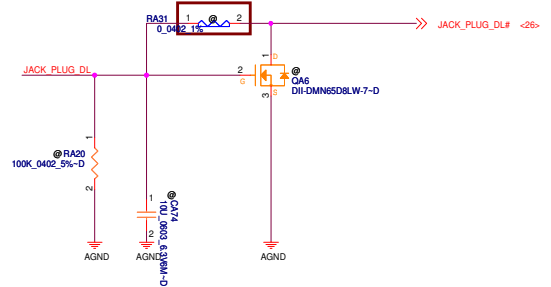
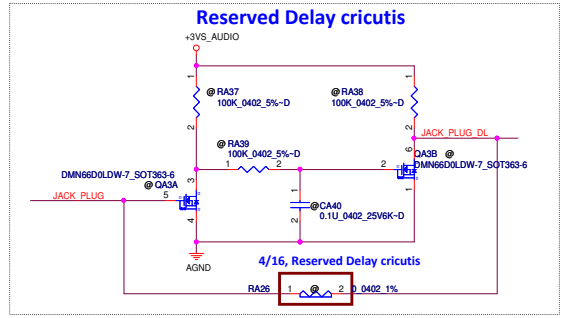
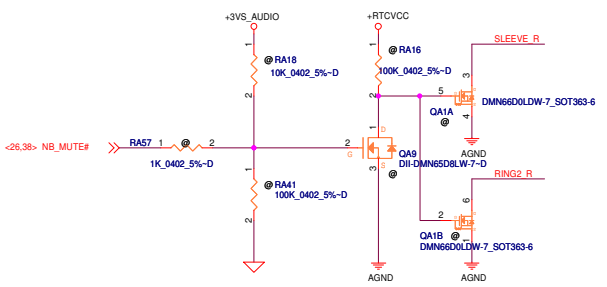


Int. Speaker Conn.



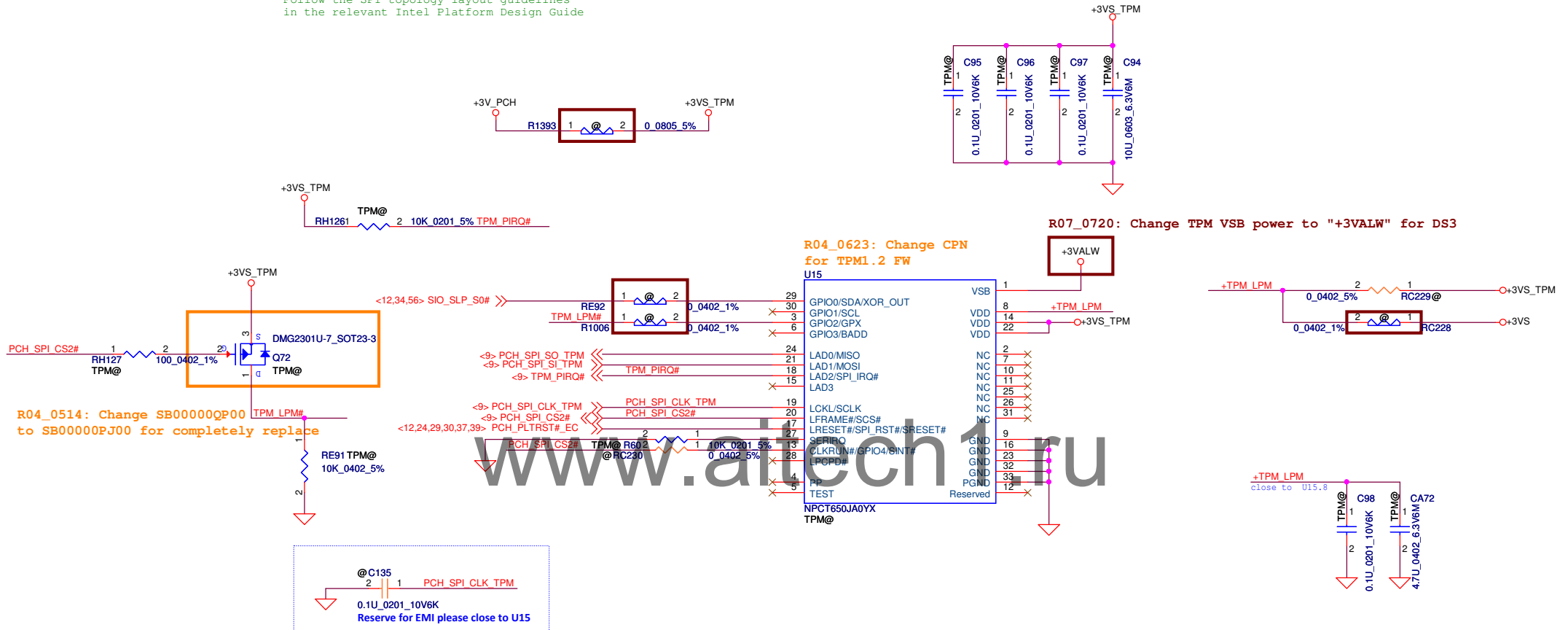
www.aitech1.ru

Prevent S3/S4/S5 Background Noise.
ALC3234/3246 has already integrated this grounding circuit inside the pin20



NOTE:
Place 0.1 uF capacitors as close as possible to the device power pins

NOTE:
Follow the SPI topology layout guidelines
in the relevant Intel Platform Design Guide

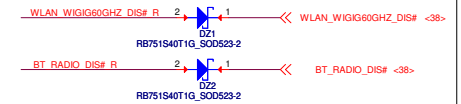
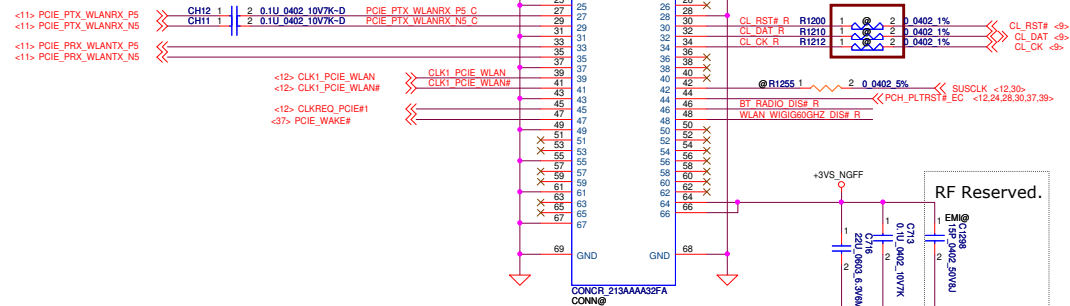
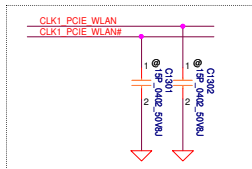
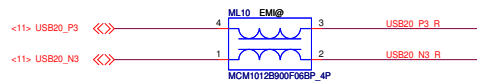


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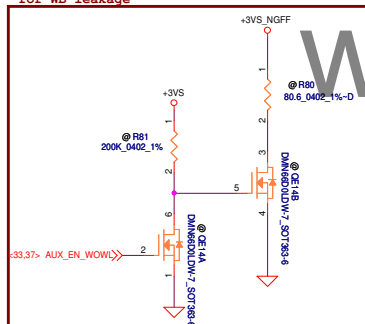
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					LA-C881P	1.0
				Date:	Tuesday, October 13, 2015	Sheet 28 of 59

M.2 Slot-A Key-A (WLAN)



R07_0731: Add +3VS_NGFF discharge circuit for WB leakage



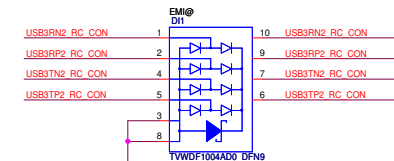
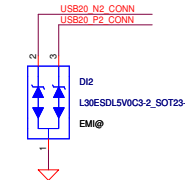
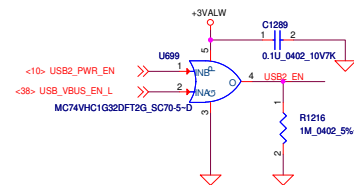
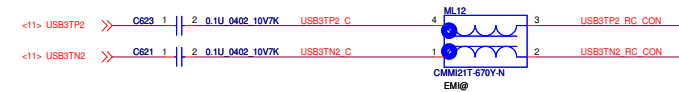
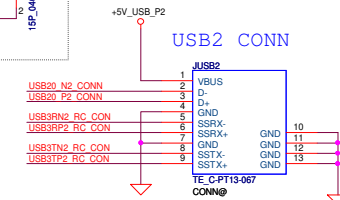
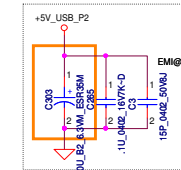
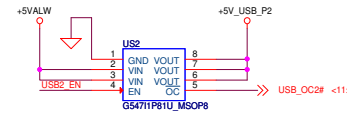
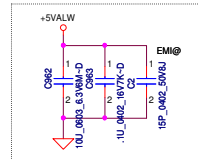


Date:	Tuesday, October 13, 2015	Sheet	30	of	59
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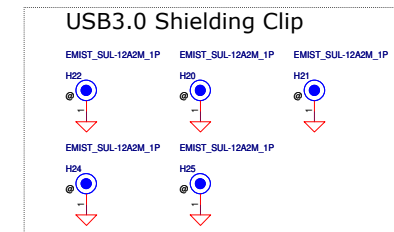
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Issued Date		2013/07/04		Deciphered Date	
				2013/10/28	
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				P30-SSD(M.2) / FAN	
				Size C Document Number LA-C881P	
Date: Tuesday, October 13, 2015				Sheet 30 of 59	

USB IO Port

R03_0429: Change from SGA00004E10 to SGA00004E00



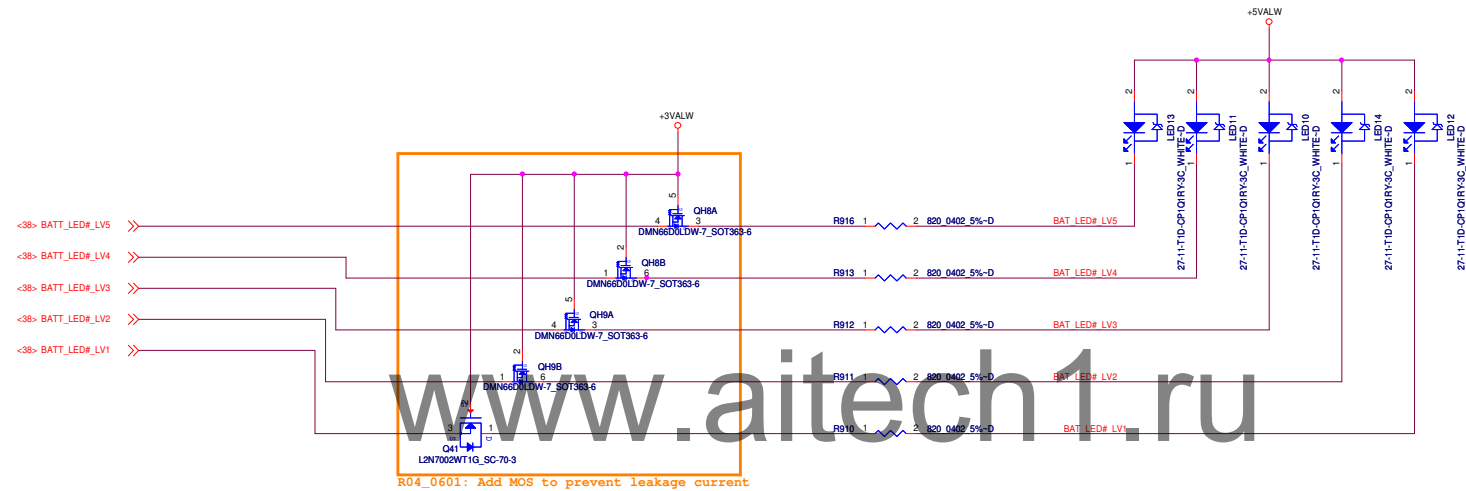
Hank0225: Note, PCB footprint is different from TVWDF1004AD0_DFN9, but it's compatible.



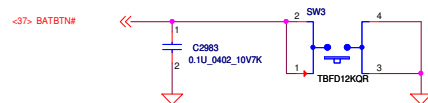
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Title <div style="text-align: right; font-weight: bold;">P31-US3.0 IO CONN</div>		Rev <div style="text-align: right; font-weight: bold;">1.0</div>	
Size Document Number <div style="text-align: right; font-weight: bold;">LA-C881P</div>		Date: Tuesday, October 13, 2015 Sheet 31 of 59	

Battery Gauge LED



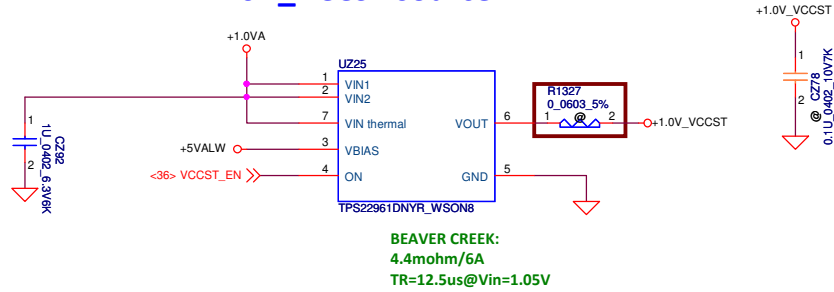
Battery Gauge Button



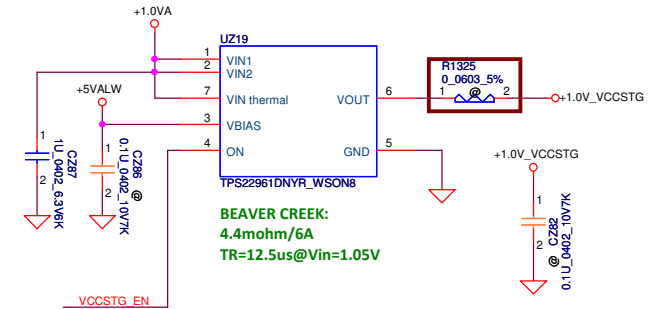
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				LA-C881P	1.0
				Date: Tuesday, October 13, 2015	Sheet 32 of 59

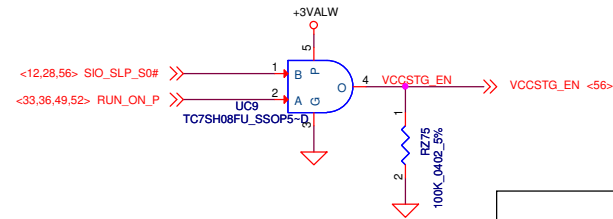
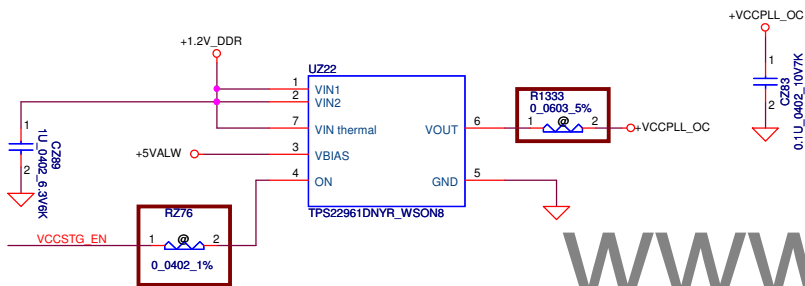
+1.0V_VCCST source



+1.0V_VCCSTG source

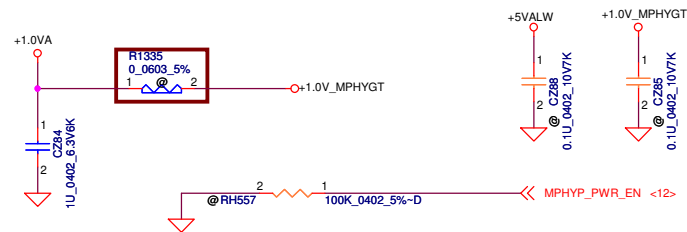


+VCCPLL_OC source

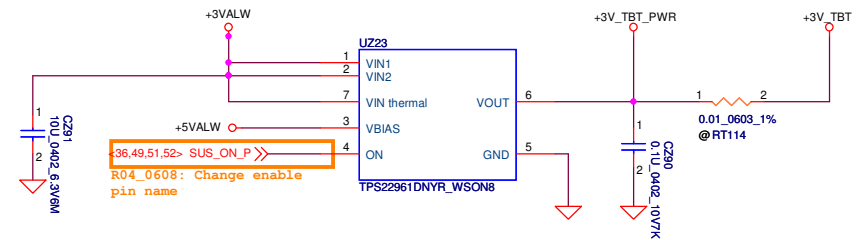


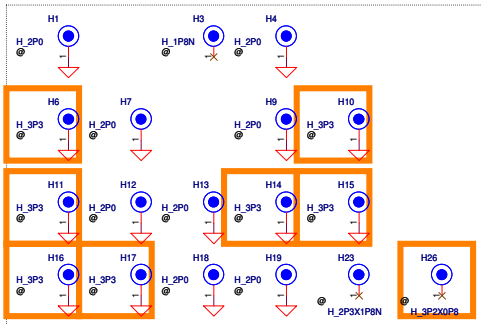
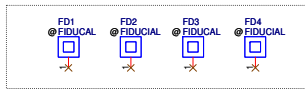
	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

+1.0V_MPHYGT source



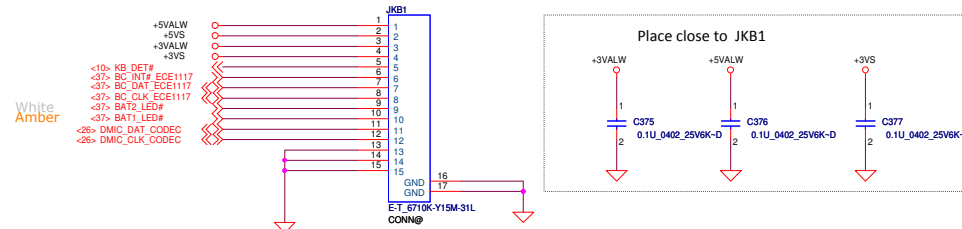
TBT Power circuits





R06_0822: Stand off screw hole change form 3.2mm to 3.3 mm.
R06_0826: Add H26 for SSD bracket.

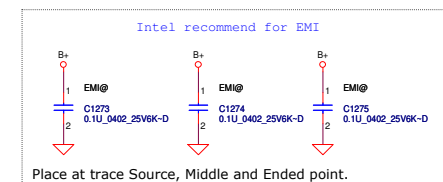
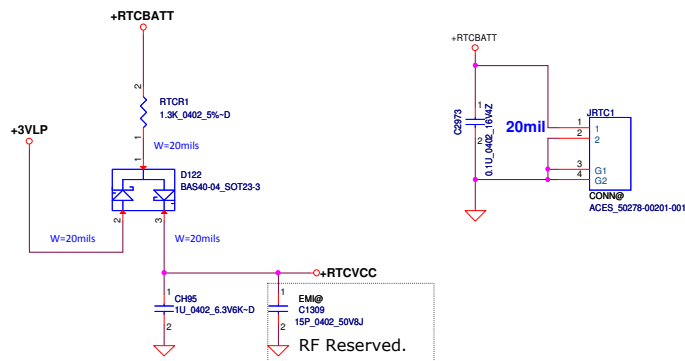
Keyboard Controller board + DMIC



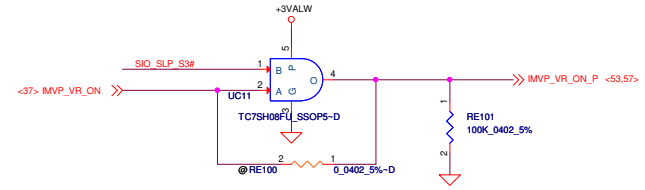
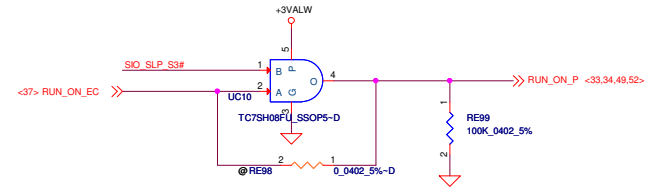
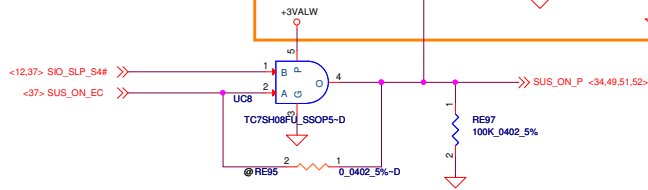
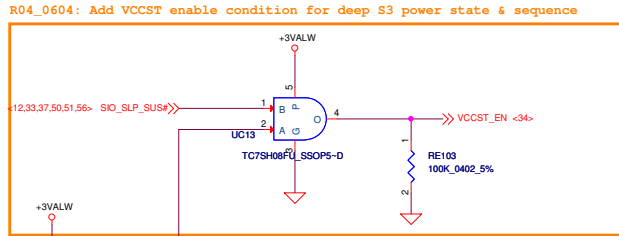
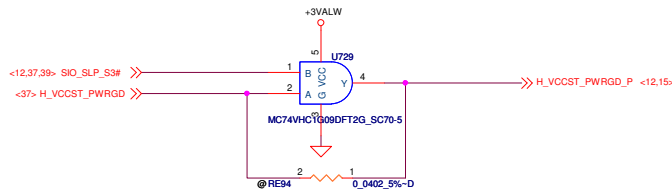
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RTC Battery With Charge Function

RTC Battery Conn

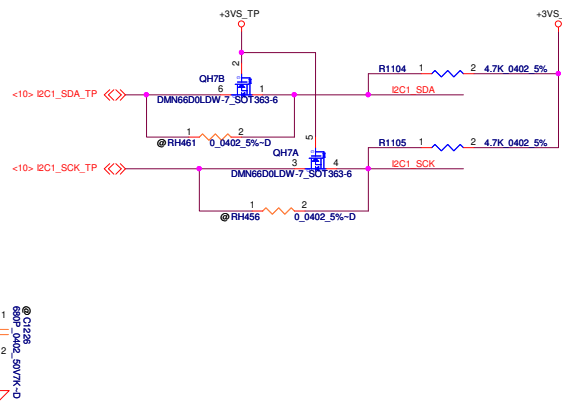
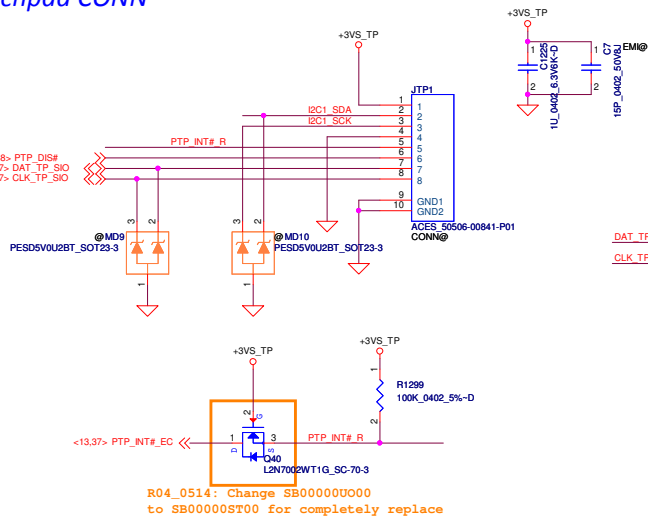


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				Size	Document Number
				LA-C881P	
				Date:	Tuesday, October 13, 2015
				Sheet	35 of 59
				Rev	1.0

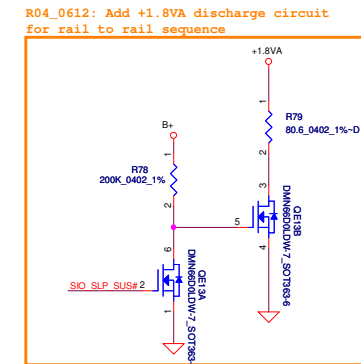


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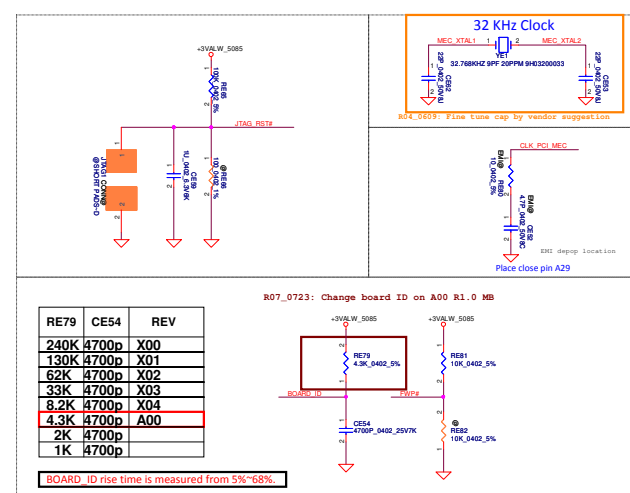
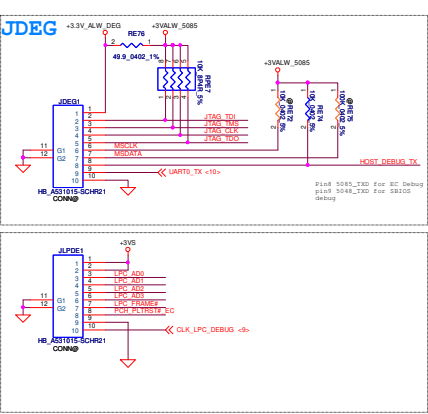
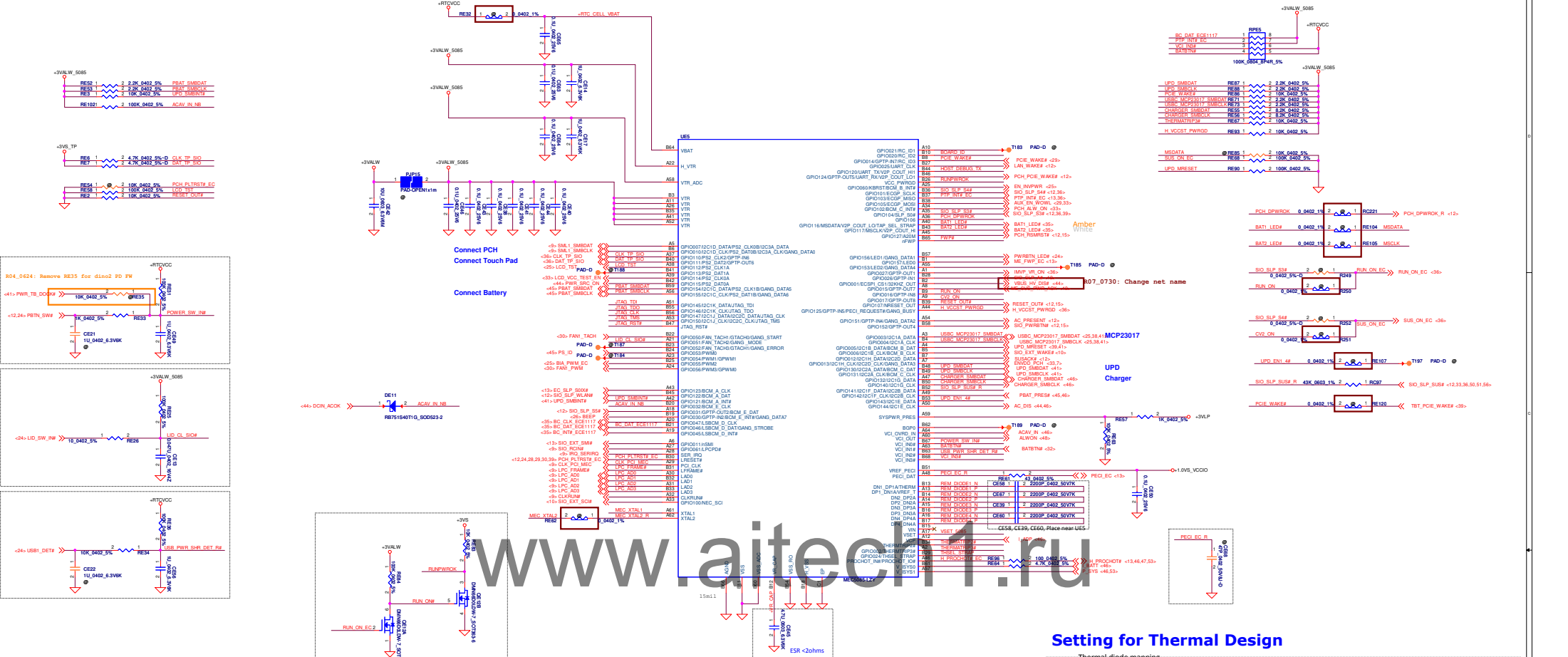
Touchpad CONN



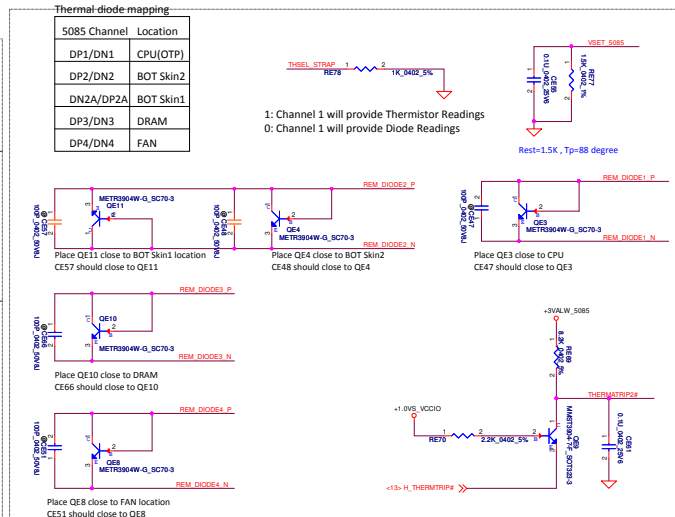
+1.8VA Discharge

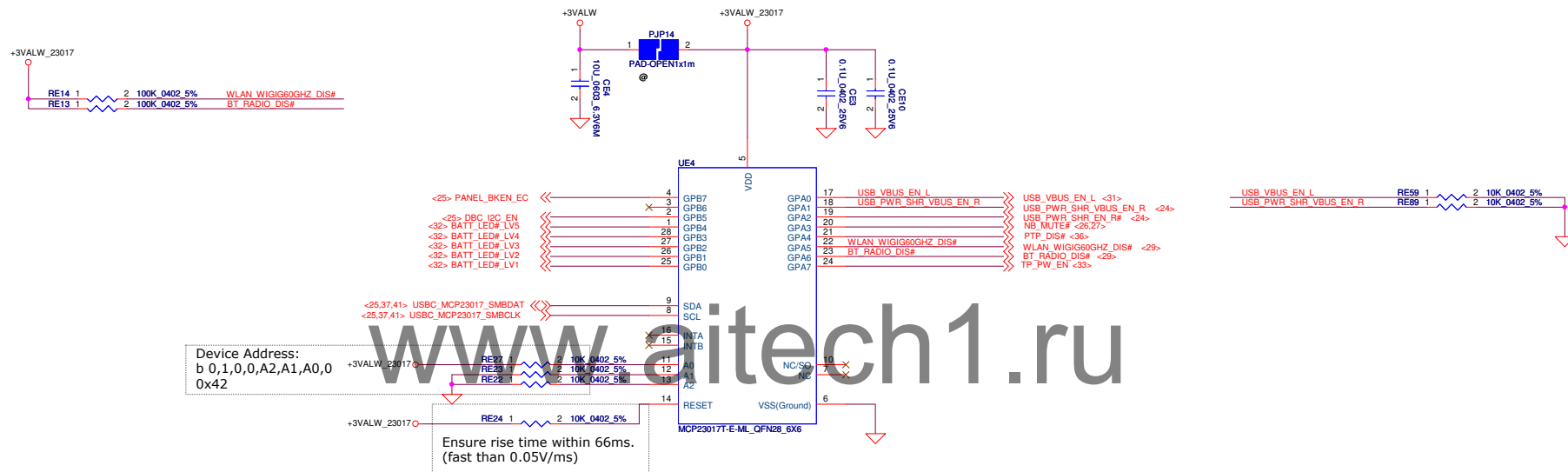


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				Document Number	
				LA-C881P	
				Rev	
				1.0	
				Date	
				Tuesday, October 13, 2015	
				Sheet	
				36 of 59	

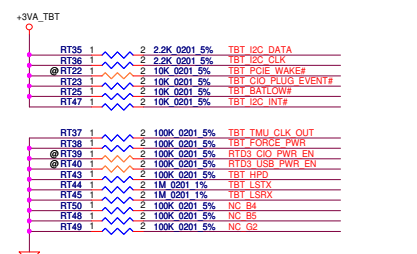
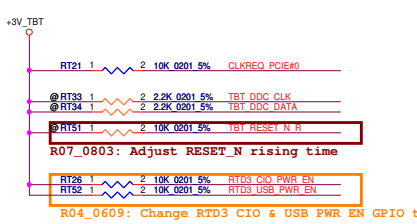
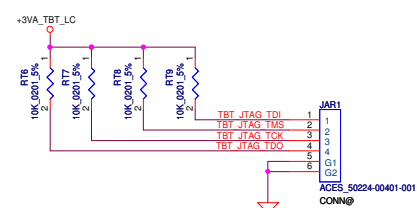


Setting for Thermal Design



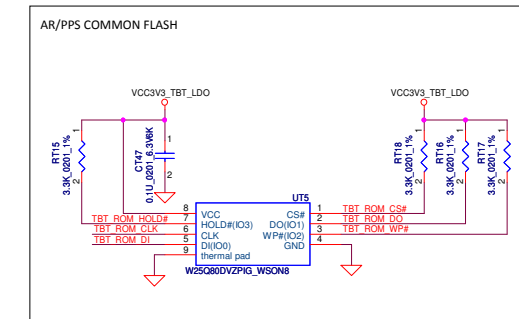
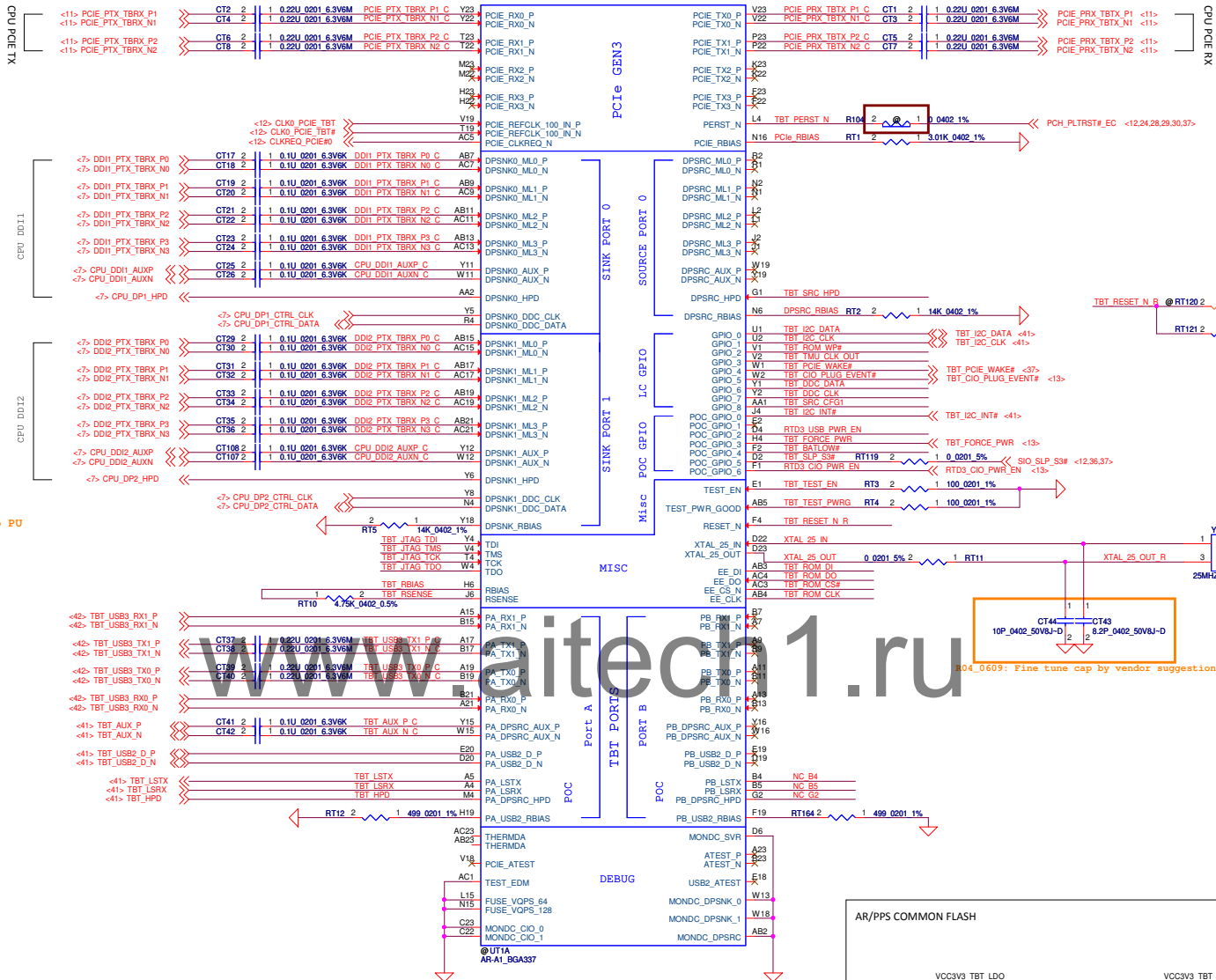


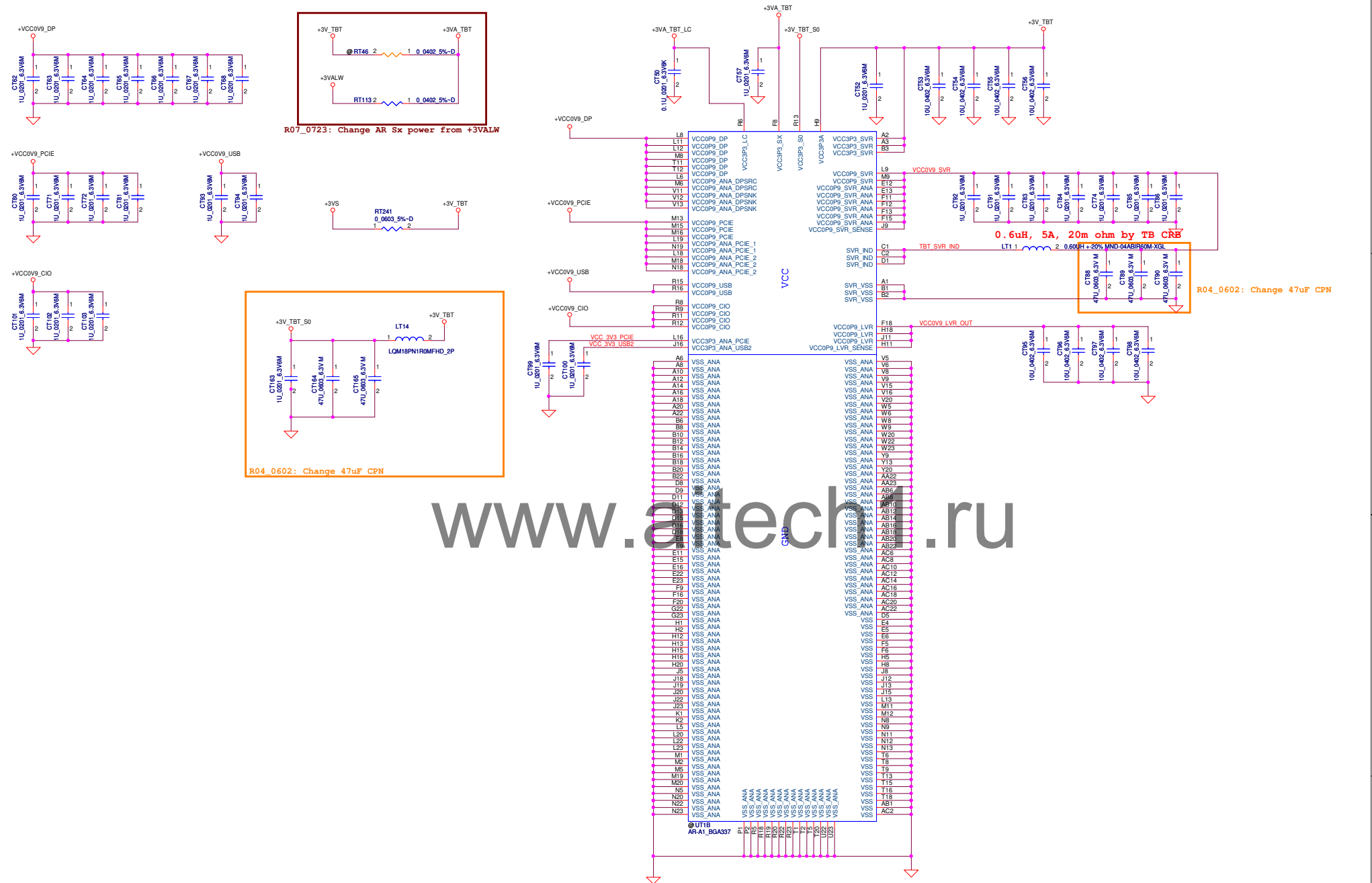
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										Document Number	
										LA-C381P	
										Date	
										Tuesday, October 13, 2015	
										Sheet 38 of 59	
										Rev 1.0	



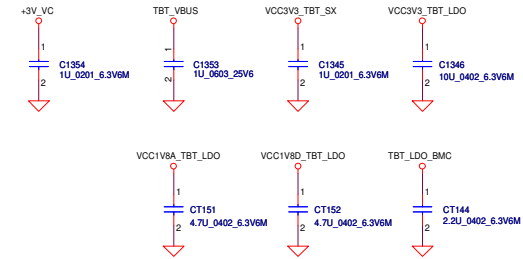
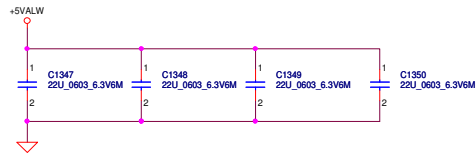
NOTE:
ASSEMBLE R297, R299 if DPSRC
NOT IN USE

TBT_SRC_CFG1 R1403 1 2 1M 0.001 1%
TBT_SRC_HPD R1405 1 2 1M 0.001 1%

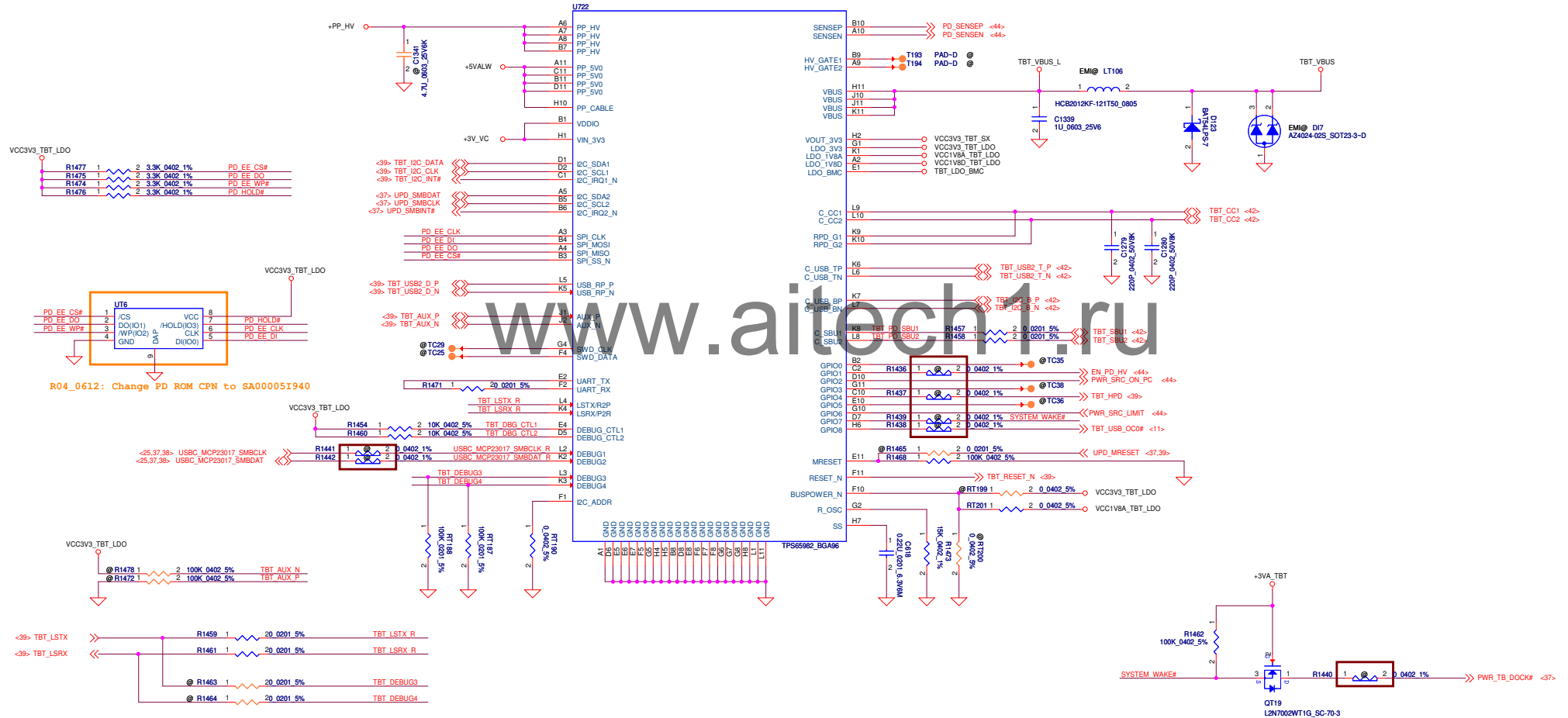


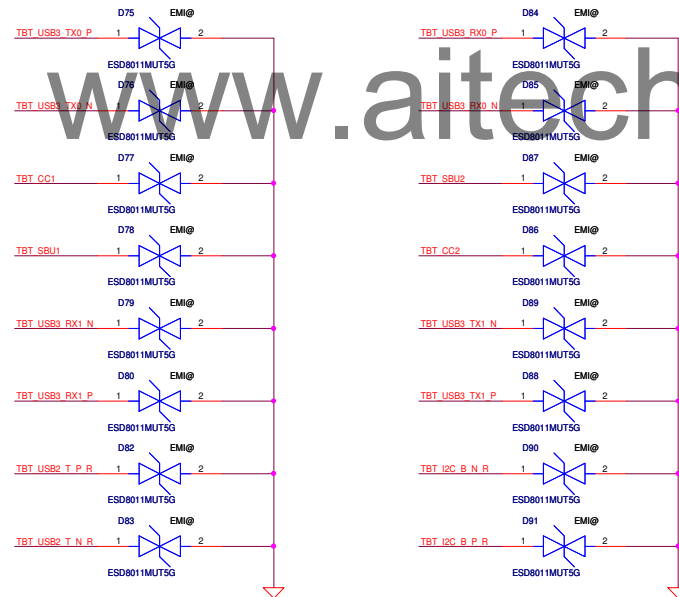
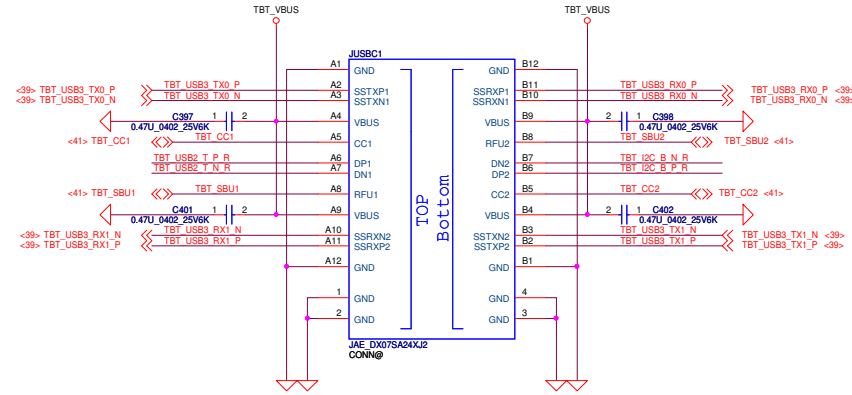
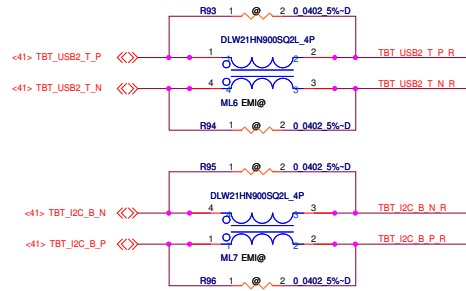


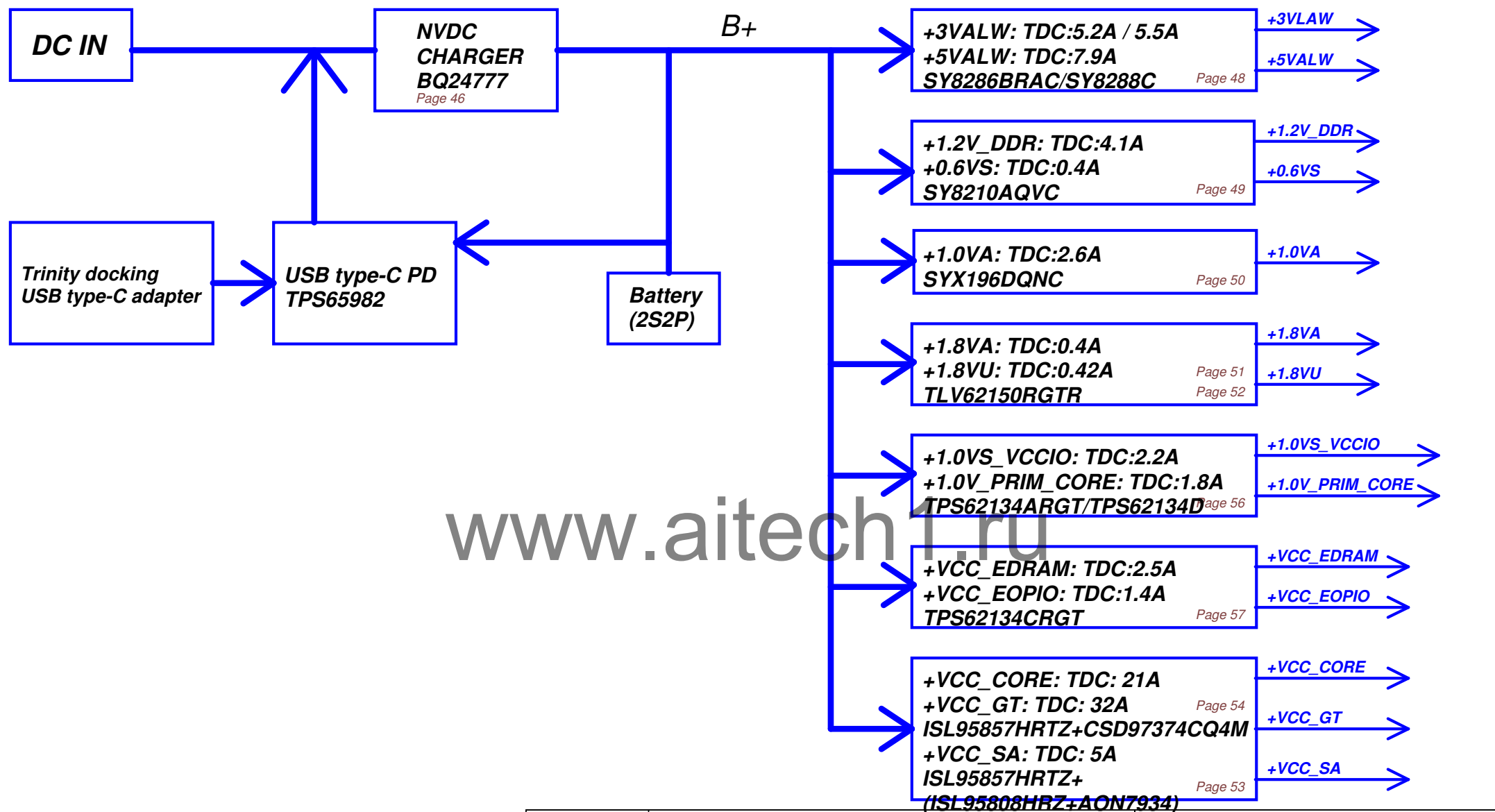
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R07_0720: Change PD to MP CPN







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				Document Number
				LA-C881P
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				Date: Tuesday, October 13, 2015
				Sheet 43 of 59

B+ Power

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Barrel Adapter

S1

S2

+SDC_IN

USB type-C Adapter

For Inrush (CTO)

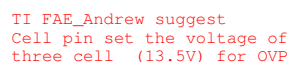
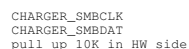
For Inrush (CTO)

Barrel_AC Detector

Vbus_AC Detector

Docking Power Control(41.1), Support component(41.2)

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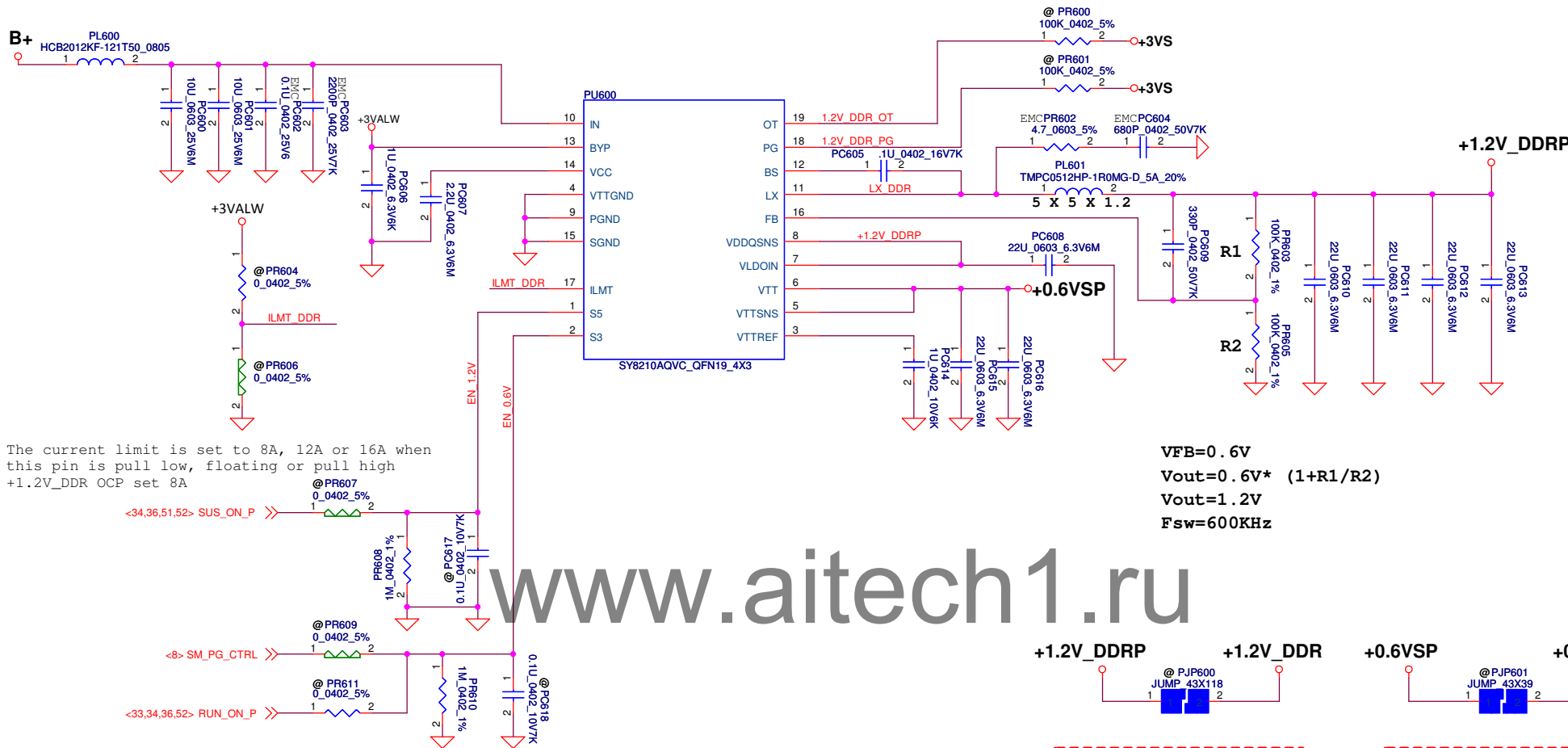
PU404_Main source
PQ409A open at 3/5V_B+ below 5.73V
and 3/5V_B+ recover 6.05V PA409A close

PU404_2nd_source
PQ409A open at 3/5V_B+ below 5.72V
and 3/5V_B+ recover 6.05V PA409A close

PU404_3rd_source
PQ409A open at 3/5V_B+ below 5.73V
and 3/5V_B+ recover 6.04V PA409A close

Component (37.1)

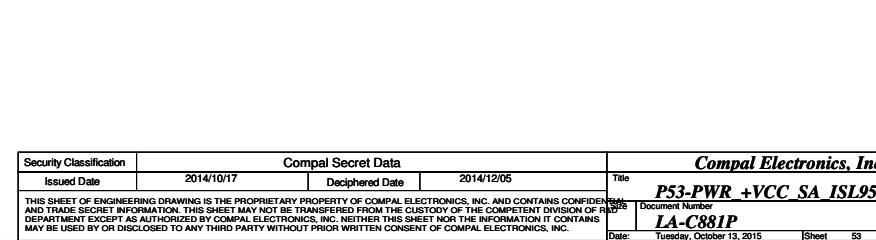
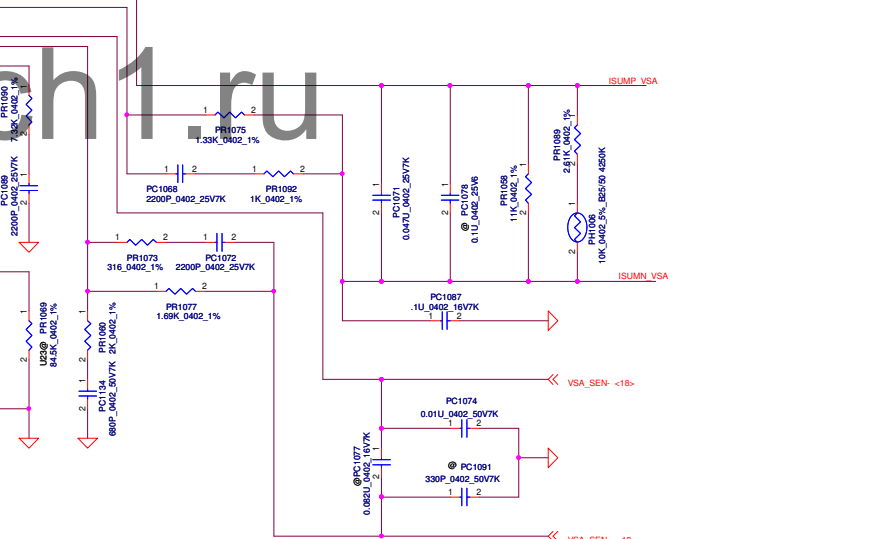
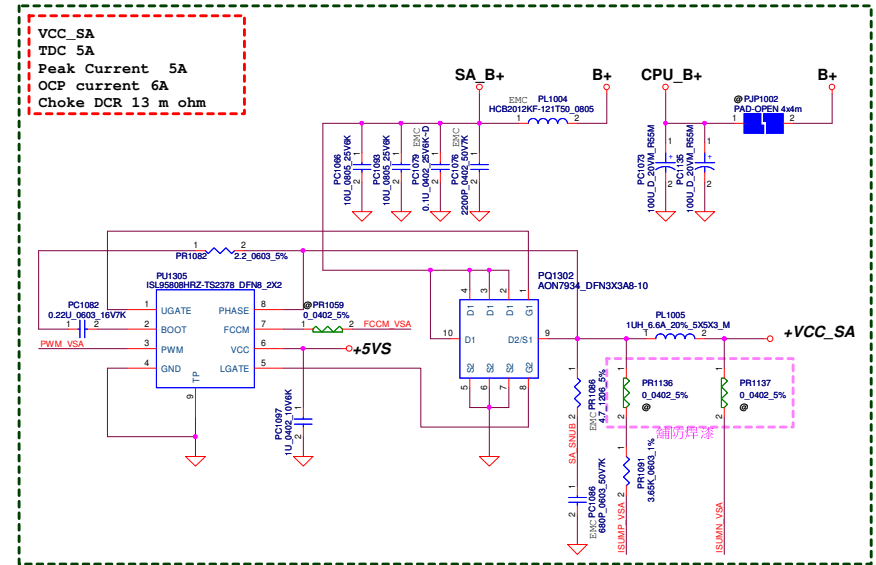
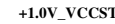
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				Document Number
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				0.4
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DDR controller(35.3), Support component(35.4)

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				Date	LA-C881P
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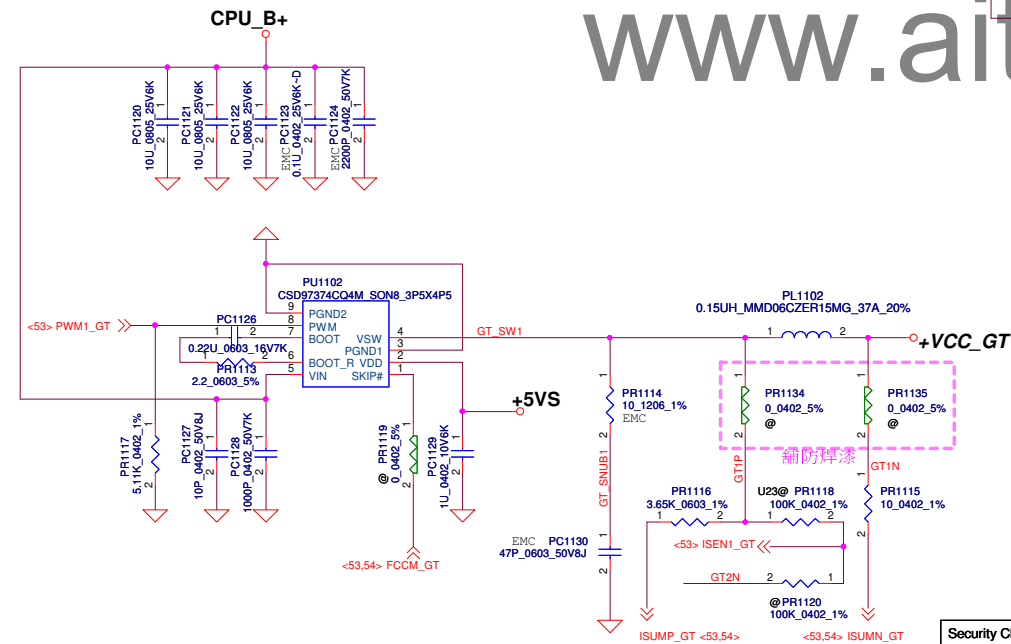
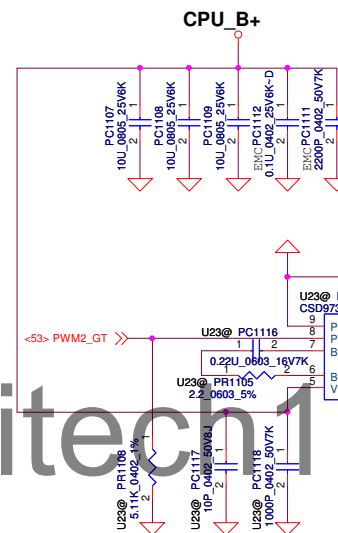
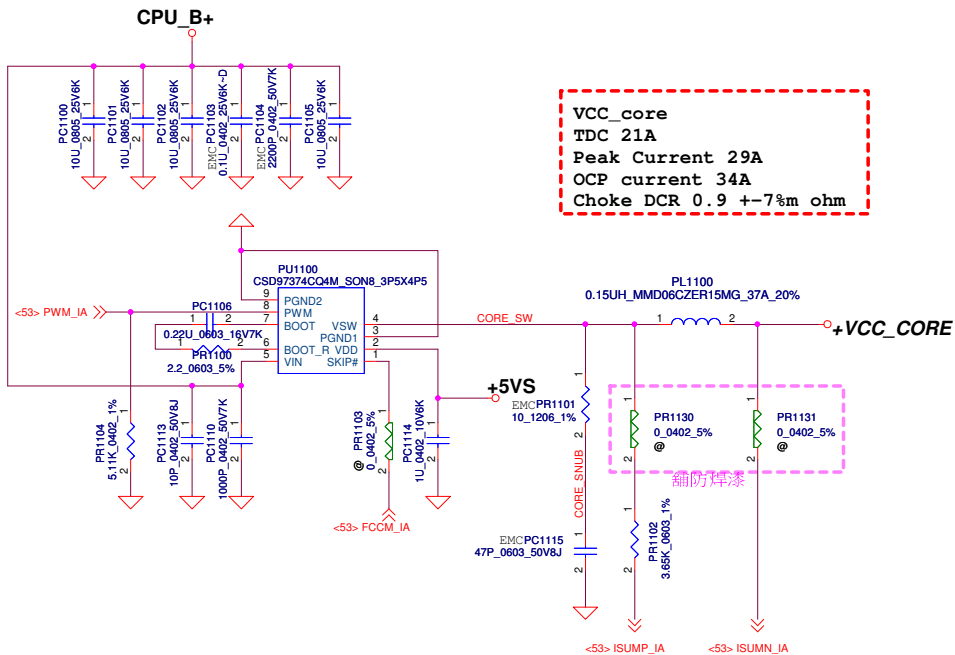
Local sense put on HW site



	U23	U22
PR1093	2.49K	1.96K
PR1088	2.61K	4.42K
PC1094	0.1U	0.047U
PC1085	0.033U	0.047U
PR1061	475	374
PR1069	84.5K	124K
PR1094	100K	78.7K

VCC_CORE controller(36.1), Drivers (36.2), Support component(36.3)

Security Classification	Compel Secret Data		Compel Electronics, Inc. Title P53-PWR +VCC SA ISL95857 Document Number LA-C881P	
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VCC_GT (U-line 22)
TDC 18A
Peak Current 31A
OCP current 37A
Choke DCR 0.9 +-7% ohm

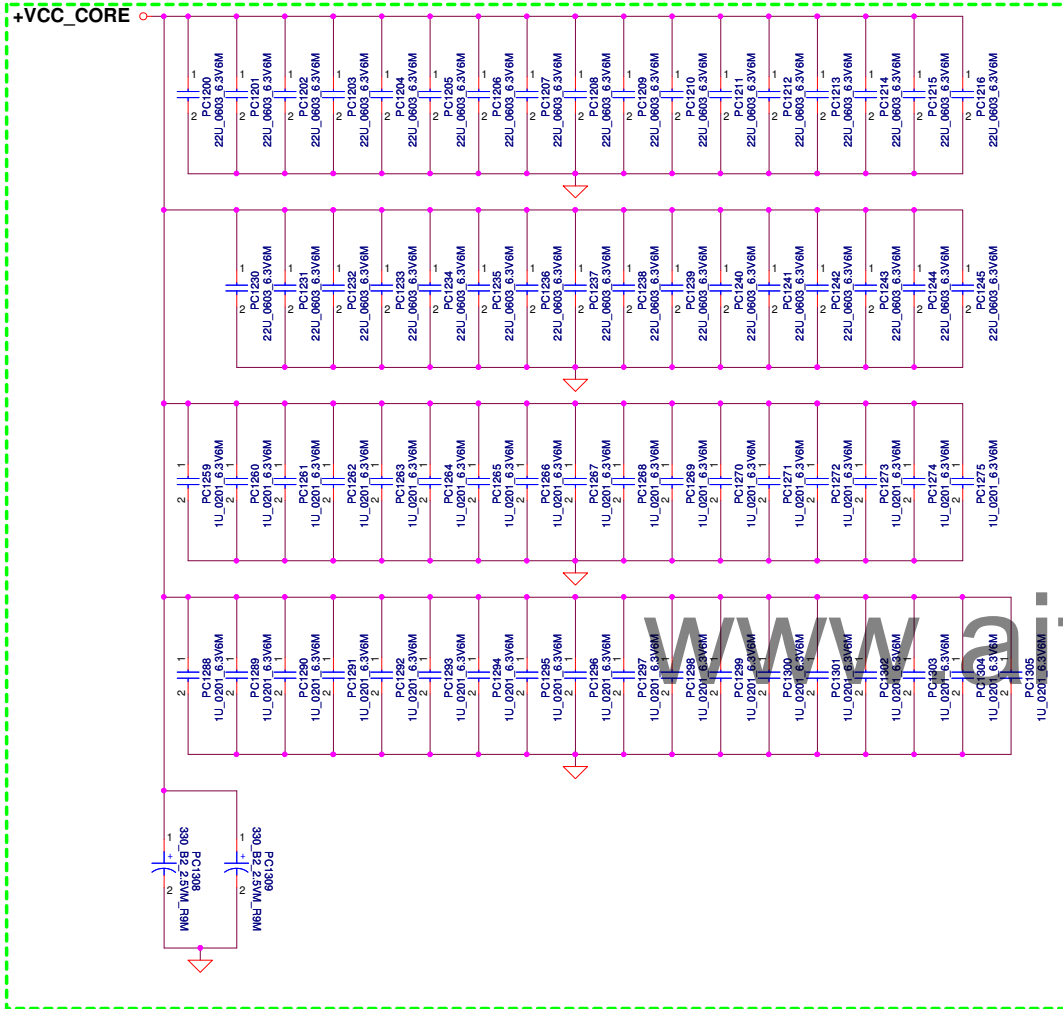
VCC_GT (U-line 23e)
TDC 32A
Peak Current 57A
OCP current 74A
Choke DCR 0.9 +-7% ohm

VCC_GTx
TDC 5A
Peak Current 7A

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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title	P54-PWR +VCC CORE/GT
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				Date	Rev
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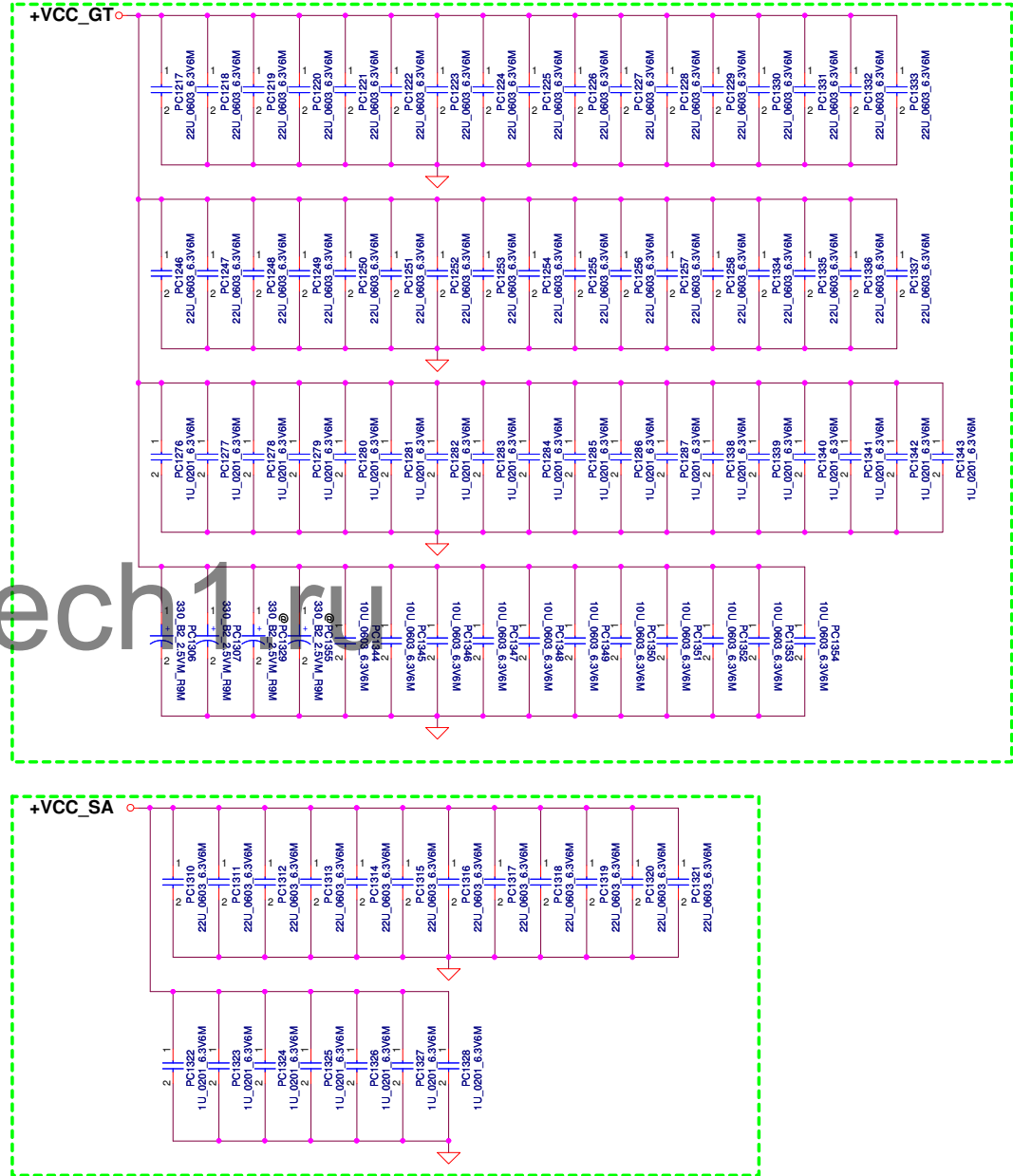
VCC_CORE Place on CPU
TOP Side.
22U_0603 * 26 pcs +1U_0201*33 pcs
Bottom Side.
330u_D2*2 pcs + 22U_0603 * 7 pcs + 1U_0201 *2



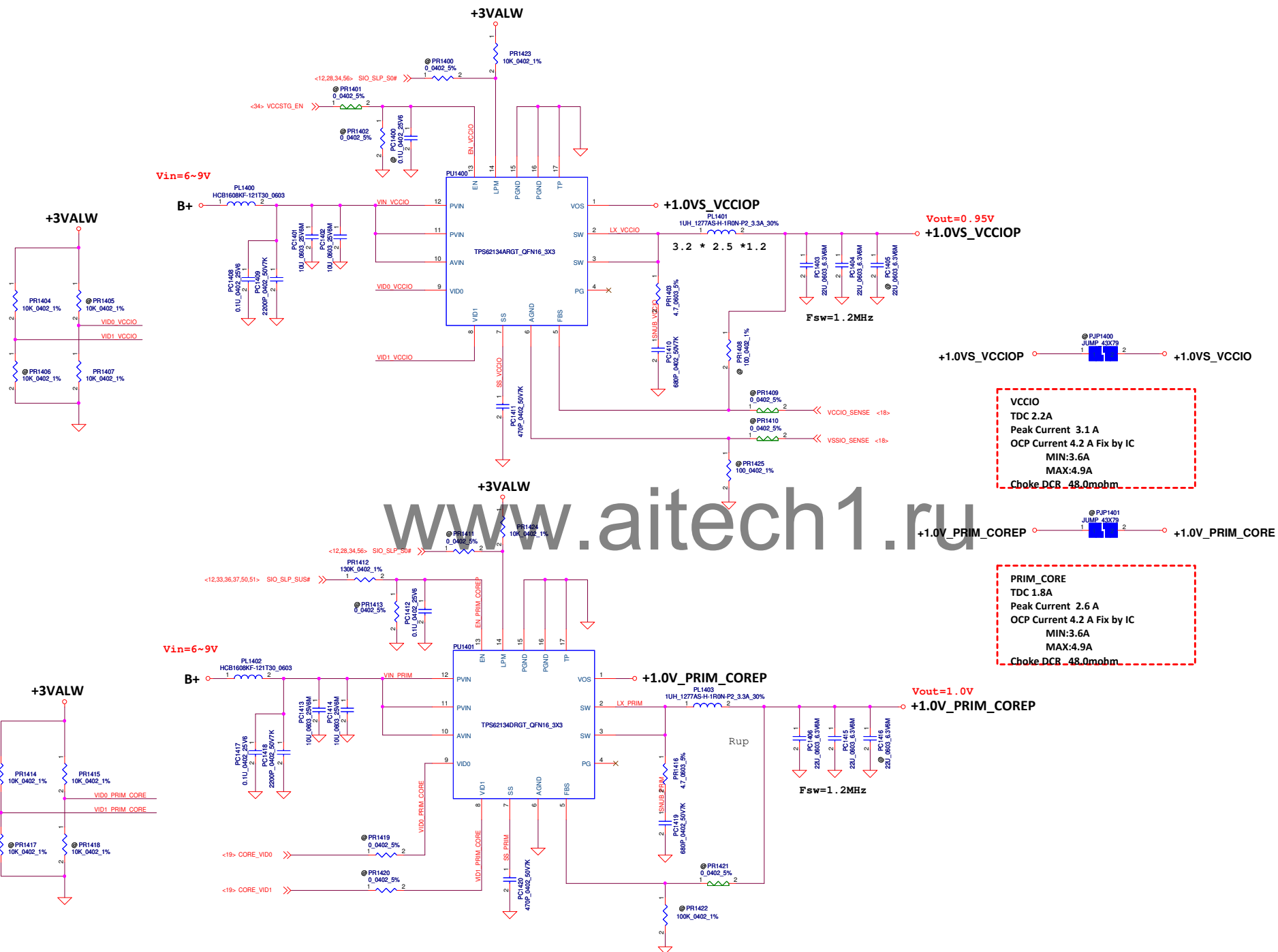
VCC_SA Place on CPU
TOP Side.
22U_0603 * 10 pcs + 1U_0201*7 pcs
Bottom Side.
22U_0603 * 2 pcs

VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6)

VCC_GT Place on CPU
TOP Side.
22U_0603 * 34 pcs +10U_0603*11 pcs +1U_0201*18 pcs
Bottom Side.
330u_B2*4 pcs



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Date:	Tuesday, October 13, 2015	Sheet	55	of	59

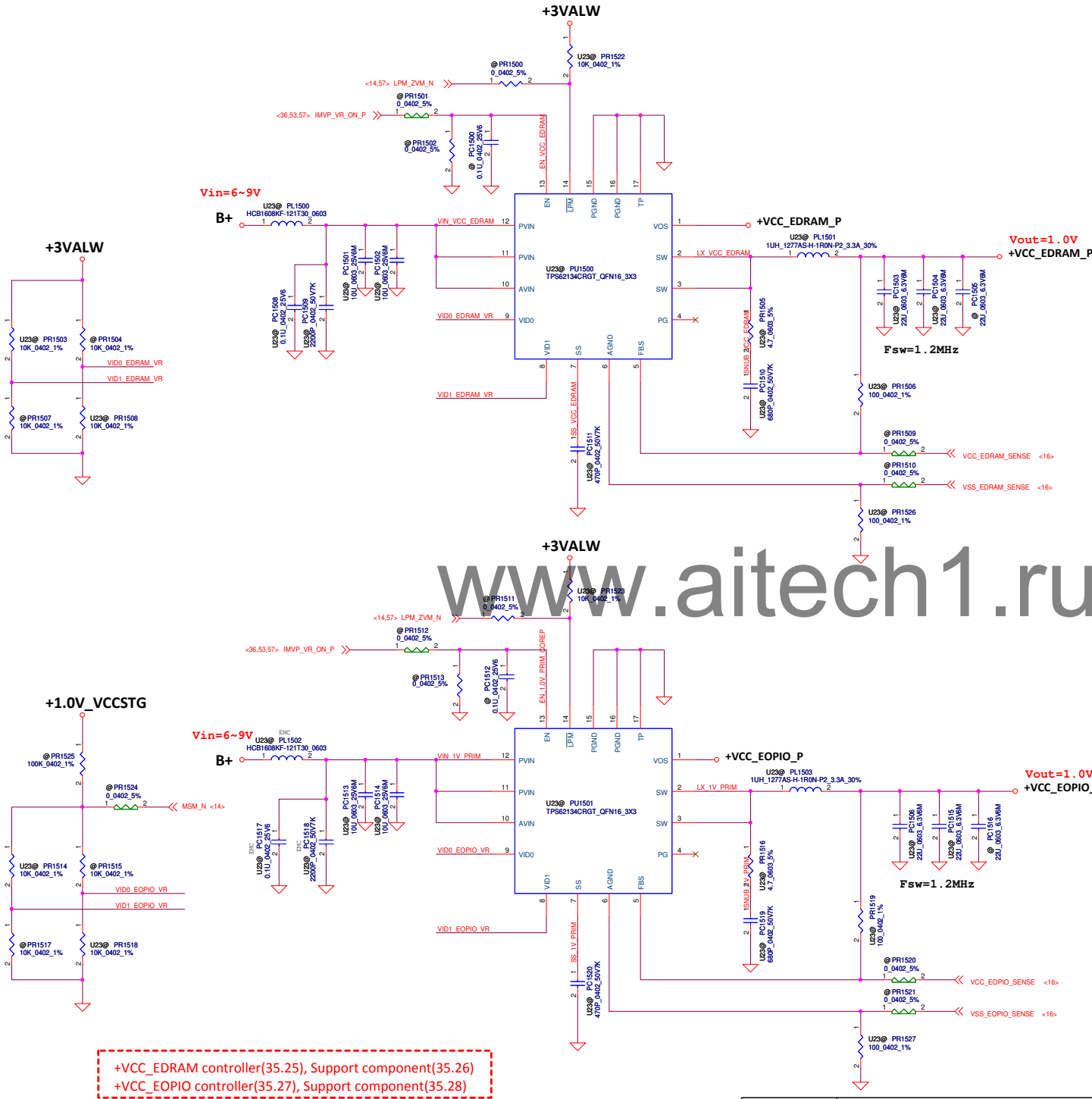


+1.0VS_VCCIO controller(35.21), Support component(35.22)
+1.0VS_PRIM_CORE controller(35.23), Support component(35.24)

VCCIO
TDC 2.2A
Peak Current 3.1 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 48.0mohm

PRIM_CORE
TDC 1.8A
Peak Current 2.6 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 48.0mohm

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				Size Document Number
				LA-C881P
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+VCC_EDRAM controller(35.25), Support component(35.26)
+VCC_EOPIO controller(35.27), Support component(35.28)

+VCC_EDRAM
TDC 1.75A
Peak Current 2.5 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 48.0mohm

+VCC_EOPIO
TDC 1.4A
Peak Current 2.0 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 48.0mohm

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P44	PQ206A	2015/09/15	Henry Chen		PQ206A change to POP	
2	P44	PU201B	2015/09/15	Henry Chen		PU201B change to NC	
3	P44	PD206	2015/09/15	Henry Chen		PD206 change to NC	
4	P44	PR236, PR238	2015/09/15	Henry Chen		PR236, PR238 change to NC	

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Timing diagram for T37. The pulse width is 1.000 μs.

135	#MVP_VR_ON	To	BYS_PWARK(RESET_OUT#)	
136	PCH_PL1TRST#	To	VCC_CORE	
137	PCH_PL1TRST#	To	VCC_GT	

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Security Classification		Compul Secret Data		Title	
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2011/06/02		2019/01/28		Compul Electronics, Inc. PS-5Power Up Sequence	
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LA-381P (LA-381P)				Rev 1 1	